AN INTEGRATED VOLTAGE-TO-FREQUENCY CONVERTER: A TUTORIAL DESIGN STUDY OF A NEW MONOLITHIC INTEGRATED CIRCUIT.

by

Justin Harry Wickens

UNITED STATES
NAVAL POSTGRADUATE SCHOOL

THESIS

AN INTEGRATED VOLTAGE-TO-FREQUENCY CONVERTER:

A TUTORIAL DESIGN STUDY OF A NEW MONOLITHIC

INTEGRATED CIRCUIT

by

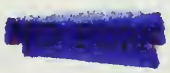
Justin Harry Wickens

June 1968

AN INTEGRATED VOLTAGE-TO-FREQUENCY CONVERTER: A TUTORIAL DESIGN STUDY OF A NEW MONOLITHIC INTEGRATED CIRCUIT

by

Justin Harry Wickens
Captain, United States Marine Corps
B.S., Naval Academy, 1960



Submitted in partial fulfillment of the
requirements for the degree of

ELECTRICAL ENGINEER

from the

NAVAL POSTGRADUATE SCHOOL
June 1968

ABSTRACT

Engineers throughout the electronics industry must understand the details of integrated circuit (IC) design, so that they can recognize possible IC applications, evaluate existing IC's, and, at times, even design new IC's. In particular, they must understand monolithic IC design, since the monolithic IC is the most prevalent IC today, and typifies IC design problems.

This thesis provides a complete introduction to monolithic IC design: circuit selection, circuit design, and circuit evaluation are discussed. Fabrication information and terminology are included as appendices. The corresponding design phases of a new IC -- the integrated voltage-to-frequency converter (VFC) -- are discussed in each section of the thesis, to illustrate the applications of the various design principles. This integrated VFC, designed by the author, is shown to be a feasible monolithic IC design.

TABLE OF CONTENTS

PAGE

APPENDIX

LIST OF TABLES

LIST OF ILLUSTRATIONS

TABLE OF SYMBOLS AND ABBREVIATIONS*

A	Voltage gain
B	Transistor base
BV	Junction breakdown voltage, as "BV_{CEO}"
C	Capacitance; transistor collector
CM	Common mode
D	Diode, as "D_1"
DM	Differential mode
E	Transistor emitter
epi	Epitaxial
f	Frequency
h_{FE}	DC current gain, $\lvert I_C/I_B \rvert$
I	Current, as "I_O"
IC	Integrated circuit
K	Kit part, as "K-1"
L	Inductance, as in "Q_L"
LV	Limiting voltage, as in "LV_{CEO}"
MV	Voltage match, as in "MV_F"
mil	10^{-3} inches (=25μ)
μ	10^{-6} meters
n	Doped n-type $\leq 10^{19}$ cm^{-3}
n+	Heavily doped n-type $> 10^{19}$ cm^{-3}
p	Doped p-type $\leq 10^{19}$ cm^{-3}
p+	Heavily doped p-type $> 10^{19}$ cm^{-3}

*Certain symbols have more than one possible meaning, but their usage is defined in the text.

TABLE OF SYMBOLS AND ABBREVIATIONS (Cont.)

P	Power dissipation, as in "P_{MAX}"
Q	Transistor, as "Q_1"; quality factor, as "Q_L"
R	Resistance
Sat	Saturation, as in $V_{CE(Sat)}$
t	Time
T	Specific time; temperature
τ	Transit time
TC	Temperature coefficient, as "TCR" ("temperature coefficient of resistance")
V	Voltage with respect to ground, as "V_1"; voltage between two nodes, as "V_{CE1}"
$\overline{V}$	Average value (DC component) of voltage, as "$\overline{V_O}$"
VCG	Voltage-controlled generator
VCO	Voltage-controlled oscillator
VFC	Voltage-to-frequency converter
Z	Impedance
$\square$	Square; i.e., length/width ratio, as "$\Omega/\square$" sheet resistance

ACKNOWLEDGEMENTS

The contributions of many people made this thesis possible. Particular credit must be given to the following:

My faculty advisors, Dr. W. M. Bauer and Dr. R. Panholzer, for their suggestions and advice.

Mr. Murray Siegel, Manager of Test Measurements and Control Applications, Fairchild Semiconductor, for the invaluable opportunity to work in his organization.

Mr. M. J. Cochran, Director of Engineering, Cintra Data Systems (formerly of Fairchild Semiconductor), for the major part of my education in IC realities, and in particular for the operational amplifier design used in this thesis.

My wife, Elizabeth, for her understanding and patient encouragement during the preparation of this thesis, and for typing most of the first draft.

1. INTRODUCTION

This thesis develops the design of an integrated voltage-to-frequency converter (VFC), as a case study in current integrated circuit* (IC) design procedures and considerations; it combines all necessary introductory information into a single tutorial example of monolithic IC design. Figure 1-1 shows the final result of the design example: the circuit breadboard for a new IC design.

Technical literature on any new development has three common characteristics: an historical sketch, illustrating the origin of the new development; an attempt to justify the importance of the new development by tabulating its advantages; and a list of definitions, which attempts to provide some order to the chaotic abundance of terminology surrounding the new development. It is perhaps indicative of the present acceptance of IC's that this paper relegates the first and last items to appendices, including them only for the sake of completeness, and does not debate the advantages of IC's at all.

Exploiting the tremendous potential of IC's today is often hampered by two factors:[1,**]

1. An apparent hesitancy towards the use of IC's, particularly linear IC's, on the part of large segments of the electronics industry; and

---

*Definitions of "integrated circuit" and related terms are provided in Appendix I.

**References are cited sequentially in each section, using arabic numerals in superscripts; all references are provided in a single listing at the end of this thesis. Footnotes, cited by superscript asterisks, are given on the same page as their citation.

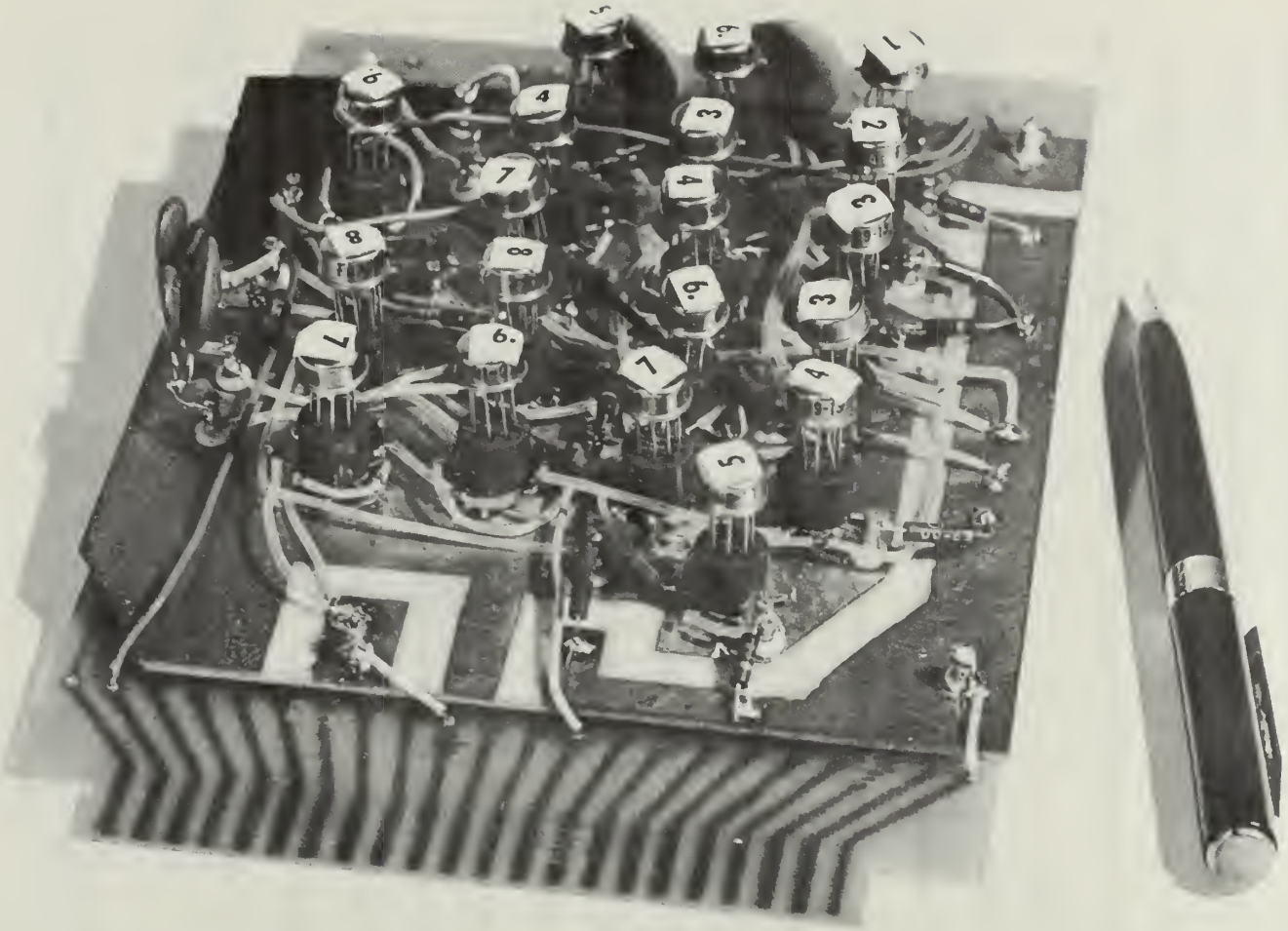


Figure 1-1: The Circuit Breadboard for the Integrated VFC.

2. The adherence of IC vendors to the production, almost exclusively, of general purpose IC's.

Both of these factors seem to stem from a mutual ignorance: potential IC users -- equipment manufacturers -- often lack sufficient understanding of IC's to properly evaluate their suitability, while IC manufacturers overlook specialized circuits which might have the same demand as more flexible designs.[2-4]

That IC's are definitely desirable and sometimes mandatory elements of many systems today is almost universally accepted.[5] Unfortunately, there is probably a large number of equipment manufacturers who cannot recognize a potential IC application when they have one; certainly very few can design their own IC's, and this design expertise may be exactly what is needed.

For instance, last year two TRW engineers described their company's development of two families of hybrid IC's for a telemetry system requirement.[6] IC's were strongly desirable for this system, but off-the-shelf IC's were unsatisfactory. Fortunately, TRW had engineers who not only understood the telemetry problem, but also were able to design suitable IC's. Such an in-house dual capability was obviously essential to the creation of an optimum system, but such capability is certainly not yet common.

On the other hand, IC manufacturers are limited by economics. Clearly volume production is essential in obtaining a low cost IC: minimum efficient production for any specific linear IC is about 100K units/year.[7] To insure sufficient sales to justify this sort of production level, IC manufacturers have concentrated almost soley on circuits which have a wide range of possible

applications, and thus a wide range of possible customers. The IC manufacturer does not usually have sufficient familiarity with specific applications areas, such as industrial control, to recognize where a special-purpose IC might have the necessary sales potential.

Mutual education is the only solution to this mutual ignorance. Potential IC users must acquire a working knowledge of IC capabilities and constraints, and some competence in IC design, which in turn require some understanding of IC fabrication. And IC manufacturers need more information on possible IC applications, so that new and probably more specialized IC's may be produced where needed. Some mutual education has already occurred, supported mainly by the IC vendors, who have tried to not only educate the rest of the electronics industry with regard to IC's, but also ascertain requirements that would lead to acceptable IC's.

The purpose of this paper is to provide some more of this mutual education. The detailed description of circuit development for the integrated VFC illustrates the problems and methodology of the IC designer, furnishing insight for potential IC users. But there is a message here also for the IC manufacturer: our IC, which is designed for a single function in a single market, portrays a radical departure from typical IC manufacturing axioms.

To be realistic we must limit ourselves to currently practical procedures and considerations. For simplicity this discussion is further limited to the common "six-mask" monolithic Silicon IC.* However, it should be noted that at present there is no single type

*A description of monolithic Silicon IC production by the six-mask method is provided in Appendix II.

of IC that can be considered "best" in all respects. In fact no single technology can provide a complete practical active IC -- even so-called "monolithic" IC's, such as the one designed here, require deposited metallization for interconnections on the chip.[8] Nonetheless, study of the monolithic Silicon IC is important since it represents the dominant technology today,[9,10] and since its capabilities and constraints are similar to those of IC's produced by the other technologies.[11]

Figure 1-2 shows the sequence of events preceding volume production of an IC.* In this thesis we will deal with the areas which normally constitute the domain of the electronic engineer: technology, specifications, circuit design, and breadboard evaluation. The necessary background information on technology is given in Appendix II; this information is widely known in the industry.

We begin this thesis by choosing specifications that give our IC -- an integrated VFC -- realistic performance requirements based on its intended market. Next, the specifications are used to select a functional configuration for the IC, under the various constraints of IC technology. Specifications and the functional configuration are covered in the next section.

The third section of this paper deals with the actual circuit design. A set of design rules is presented, and contemporary practice in linear IC design is examined. Then the circuit design for the integrated VFC is formulated.

---

*After King and Stern.[12]

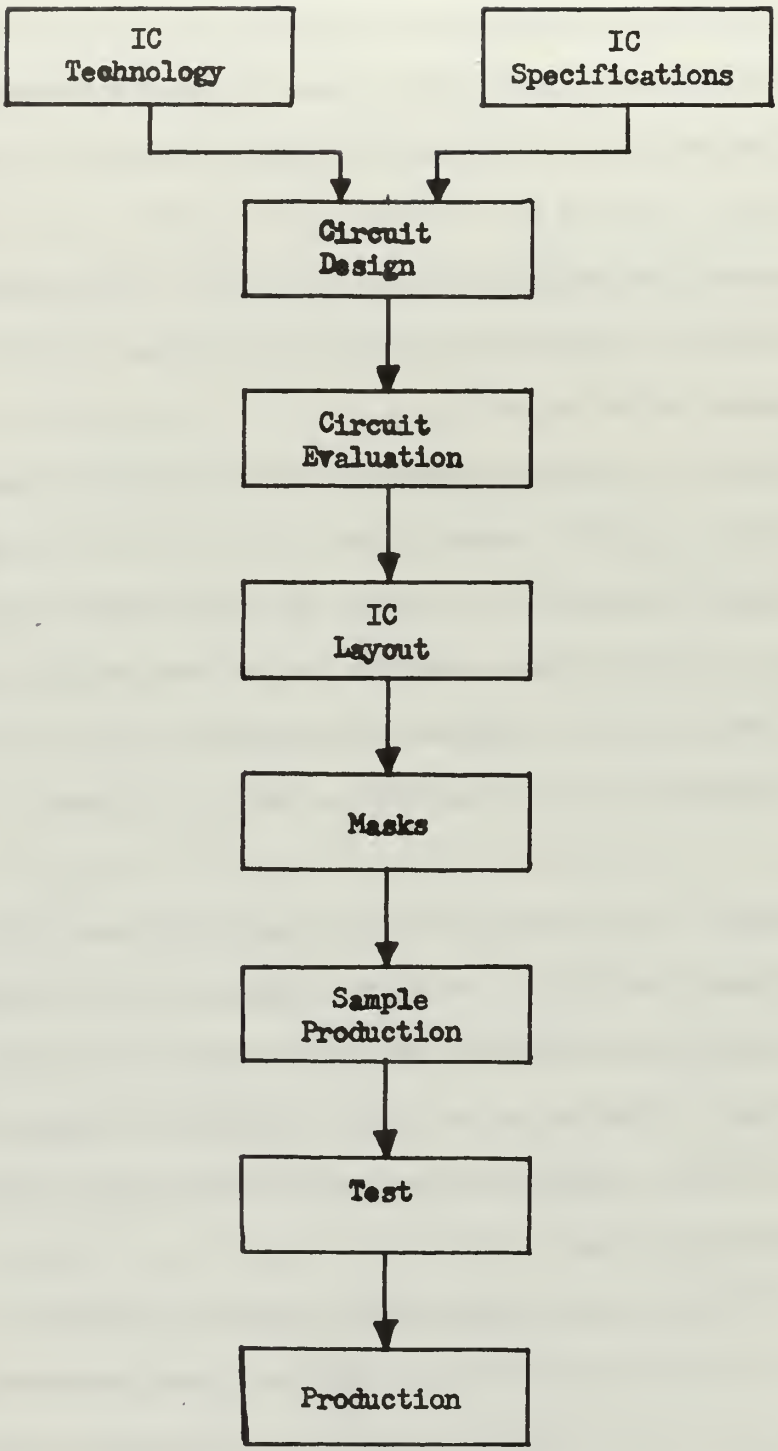


Figure 1-2: Development of an IC.

In the fourth section the design is evaluated. A breadboard version of the circuit was constructed, using actual monolithic IC active devices, and its performance was measured. The results of this evaluation are tabulated. Next, a rough circuit layout is given to demonstrate the feasibility of realizing the circuit in monolithic form on a chip of moderate size. This completes the usual role of the electronics engineer in IC design.

Because our primary purpose is to explain IC design procedures and considerations, much of the information contained in this paper is tutorial, and most of it has been published before. However, by combining diverse information in a single treatment of IC design, and by using the design of a new IC -- the integrated VFC -- as an illustration, it is hoped that this paper will provide assistance to the reader who might have occasion to use or design an IC.

2. CIRCUIT SELECTION

Linear voltage-to-frequency conversion is a common requirement in many forms of signal processing. Naturally, the form of a VFC is dictated by, among other things, the application for which it is intended. Our integrated VFC is primarily designed for use in industrial control systems.

In this section we consider the various factors that lead to the final choice of a functional configuration for our integrated VFC. First, we examine the various VFC applications, with emphasis on industrial control requirements. Next, pertinent theoretical aspects of the VFC are discussed. Then we consider existing schemes for realizing VFC's. And, finally, the functional configuration for the integrated VFC is selected.

The terms "VFC" and VCO" sometimes cause confusion. Here we use "VCO" (voltage-controlled oscillator) for a basic oscillator circuit whose output frequency varies with some controlling voltage. We reserve "VFC" for a circuit which produces a periodic output signal for a slowly varying (essentially DC) input signal, so that output frequency is directly proportional to input voltage level. Thus a VFC could be composed of a VCO, plus additional circuitry to linearize the voltage-frequency transfer characteristic.

A VCO may in general have any periodic output waveform, but usually the output is either discrete (i.e., pulses) or sinusoidal. The next section shows why the pulse output is preferable for the industrial application we have in mind. It should also be noted that, compared with a sinusoidal-output VCO, a pulse-output VCO usually is simpler and easier to reproduce in quantity, and has

wider frequency range and better linearity.[1] For these reasons we require a pulse output of our integrated VFC, and restrict the terms "VFC" and "VCO" in this paper to circuits with pulse outputs, unless some qualifying adjective is used, as in "sinusoidal VCO".

VFC APPLICATIONS

Modern industrial control systems can be characterized by the model in Figure 2-1.

The sensor output is typically a slowly varying voltage waveform, related to the process variable being measured. The channel is normally noisy, so the sensor output signal is clearly a poor choice for transmission. A binary waveform, with its significant noise immunity, is an excellent choice. However, the binary waveform must be modulated to carry the process variable information. Here a VFC is one obvious possibility for the transmitter. Figure 2-2(a) illustrates such an application; as shown, a simple frequency meter provides a good way to regain the original signal.

Moreover, process variable information may be needed in digital form: digital "linearizing"* is sometimes preferable to its analog equivalent;[2] also, the controller may include a digital computer. Happily, a VFC lends itself readily to analog/digital conversion; as shown in Figure 2-2(b), all that is needed is a counter with appropriate gating. This is one way currently used to build inexpensive digital voltmeters.[3]

*"Linearizing" here means conditioning signals to remove the information distortion caused by sensor nonlinearities.

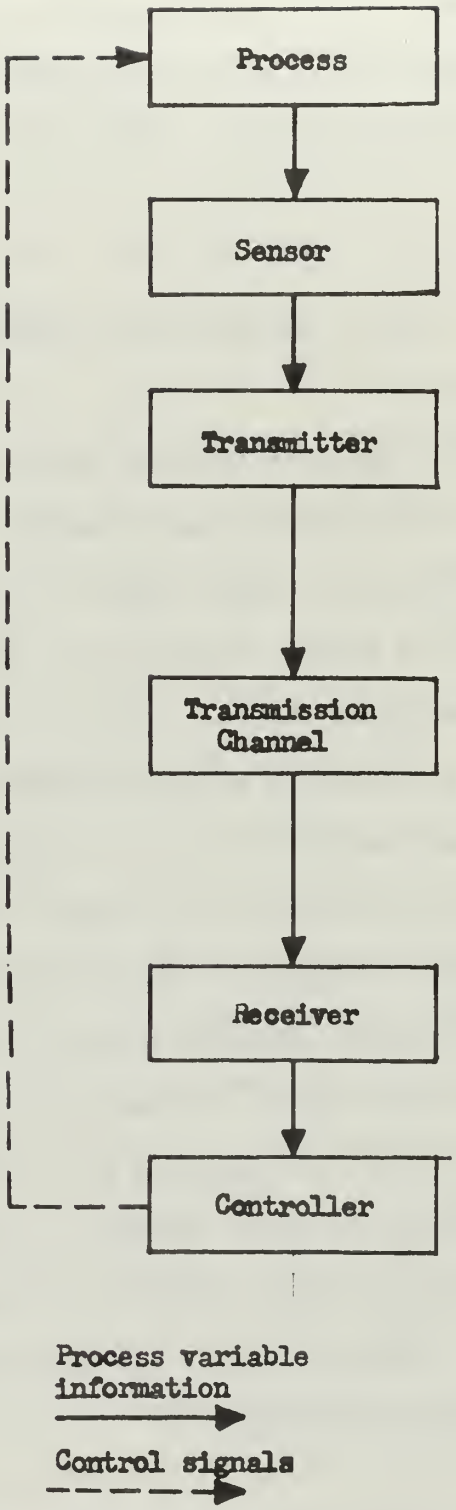
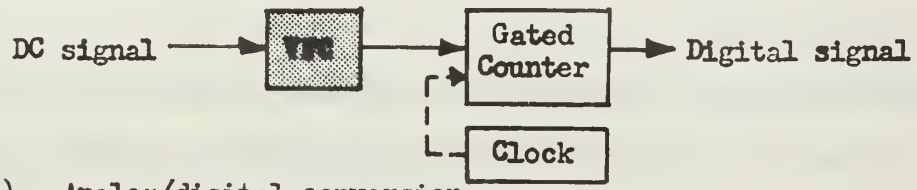
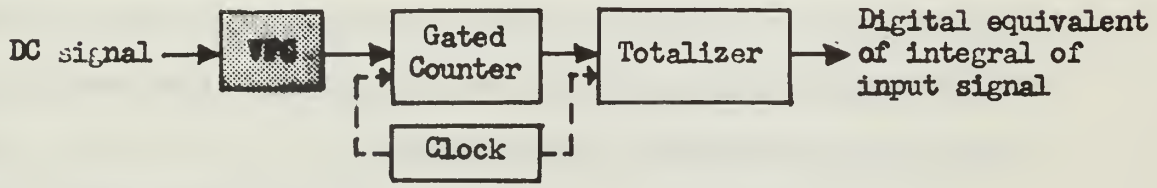


Figure 2-1: An industrial control system model.

(a). Simple pulse-frequency modulation/demodulation scheme.

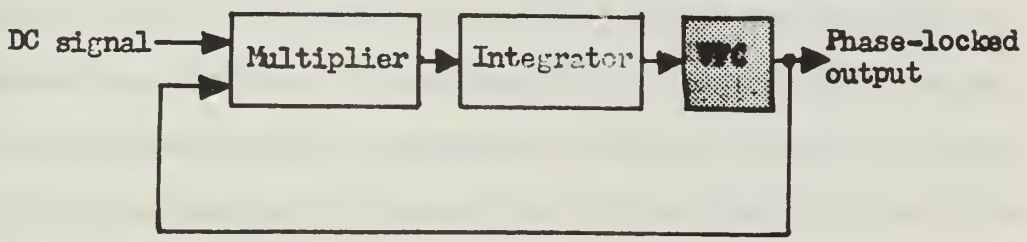


(b). Analog/digital conversion.



(c). Digital integration.

(d). Sinusoidal-output swept oscillator.



(e). Phase-locked loop.

Figure 2-2: VFC applications.

Our integrated VFC is designed for the above applications: analog/digital and analog/binary conversion in industrial control systems. Such systems typify the omnipresent compromise between cost and precision. Sensor accuracy is normally on the order of .1%*, so it is unnecessary, as well as expensive, for other components in the control system to have tolerances much less than this.

The gated counter mentioned above indicates events per unit time: the number of pulses received from the VFC in a fixed interval. If the counter is followed by a circuit which maintains a running total of counter outputs, the result is digital integration. This arrangement, Figure 2-2(c), has several uses; for example, chemical analysis and gas chromatography.[4]

Swept oscillators are used in signal simulation for circuit testing, and in signal analysis and identification. If a sinusoidal output is desired, and the frequency range is less than twice the lowest frequency, a VFC may be used with a single low-pass filter, as in Figure 2-2(d).

Frequency modulation (FM) is just another term for voltage-to-frequency conversion. In this paper we will use "FM" and "voltage control of output frequency" synonymously. Any monolithic IC, including our integrated VFC, is limited to low frequencies by parasitic effects. However, even low frequency FM has its uses. For example, sub-carrier FM in telemetry involves frequencies usually well below 1 MHz; the maximum Inter-Range Instrumentation Group standard subcarrier frequency is below 81 KHz.[5]

---

*Cf. for example, BLH Electronics, Inc. product data on S-4 strain gages.[6]

Phase-locked loops are used to derive a waveform which is at the same frequency as, and in phase with, some periodic signal. A typical phase-lock loop is illustrated in Figure 2-2(e); the VFC output may be filtered if a sinusoidal derived waveform is desired.

The examples mentioned above show the wide applicability of a VFC. The industrial control applications, with their wide tolerance and low frequencies, represent the best initial design objective for an integrated VFC.

THEORETICAL BACKGROUND

As pointed out in the preceding section, VCO's and VFC's have numerous important applications. In order to select a type of VCO or VFC for a given application, it is certainly helpful, if not mandatory, to have an exhaustive list of possible circuits from which to choose. In this section we will construct, in rough form, this categorization.

Unfortunately, there is little unified theory behind the VCO and the VFC. In fact, there is little unified theory for oscillators in general. Much has been written concerning VCO's and VFC's, and much more has been written about oscillators, but the approach invariably is to consider a specific circuit, chosen by trial-and-error engineering for a unique application, and analyzed by some method which lends itself readily to the circuit under consideration. Thus there is very little common basis for comparison of dissimilar circuits.

Edson[7] classified oscillators as harmonic or relaxation types: harmonic oscillators with nearly sinusoidal outputs and relatively

stable output frequencies, as opposed to relaxation oscillators with decidedly non-sinusoidal outputs and frequency drift problems. However, this is a classification by degree rather than type: Edson points out that there are many oscillators which defy definite assignment to either the harmonic or relaxation groups, and that any particular circuit can be a relaxation or harmonic oscillator depending on the relative magnitude of its parameters.[8]

In his doctoral dissertation, Hachtel[9] made an exhaustive classification of oscillators based on energy storage. He concluded that there were twelve possible types of oscillators; his listing is given in Table 2-1.* This classification is certainly more helpful than Edson's harmonic and relaxation categories.

However, to retain a degree of simplicity in these remarks, we postpone a closer look at Hachtel's list until the next section; here we examine oscillators, VCO's and VFC's from a simpler, though cruder viewpoint.

A basic oscillator, Figure 2-3(a), consists of a circuit which converts a portion of energy supplied to it into an output signal which has a periodic waveform. Typically, energy is supplied in the form of DC power. The output signal is often, but certainly not necessarily, a sinusoid or pulse train. In the oscillator circuitry there are always a number of parameters, and at least one voltage or current reference, which determine the operating

*Hactel excludes opto-, thermo-, and piezo-electric energy storage mechanisms from consideration.

Table 2-1

TYPES OF OSCILLATORS[a]

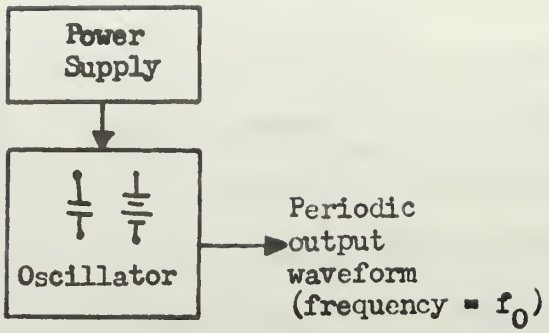
Type [b]	Energy Storage [c]	Output Frequency Relation [d]
RC Phase Shift	D, E	$f_{OSC} = K/RC$
IC Negative Resistance	I, E	
IC Phase Shift	D, I, E	
RI Phase Shift	D, I	
Transit Time	I	$f_{OSC} = K/\tau$
LC Negative Resistance	E, M	$f_{OSC} = K/(LC)^{1/2}$
LC Phase Shift	D, E, M	
RL Phase Shift	D, M	
IL Phase Shift	S, I, M	
IL Negative Resistance	I, M	
ILC Negative Resistance	I, E, M	
ILC Phase Shift	D, I, E, M	

(a) After Hachtel.[9]

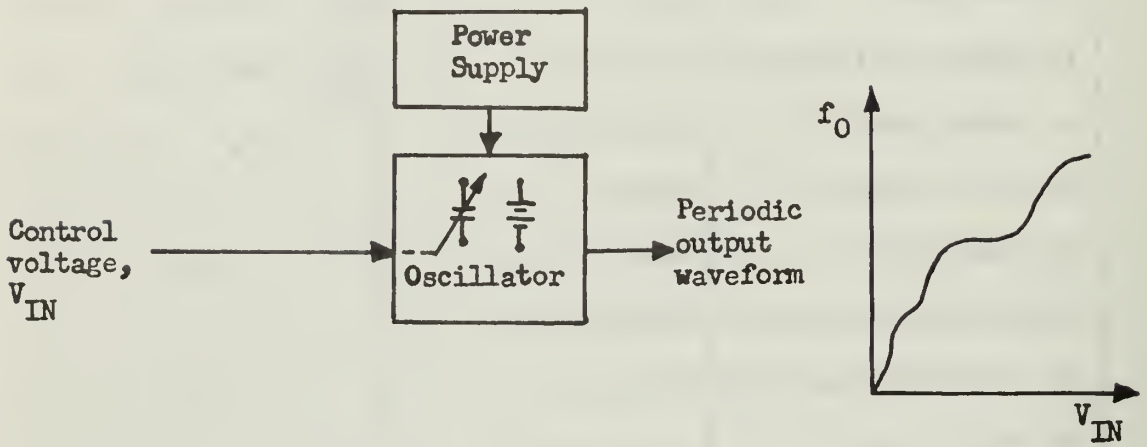
(b) Oscillators with D-type energy storage are usually formed with two-port active devices, hence "phase-shift". Oscillators without D-type storage are usually formed with one-port devices, hence "negative-resistance".

(c) Energy storage regions:
- D Dependent source regions (i.e., actual storage elsewhere).
- I Inertial energy storage (in energy of mobile charge carriers).
- E Electric field energy storage (e.g., capacitance).
- M Magnetic field energy storage (e.g., inductance).

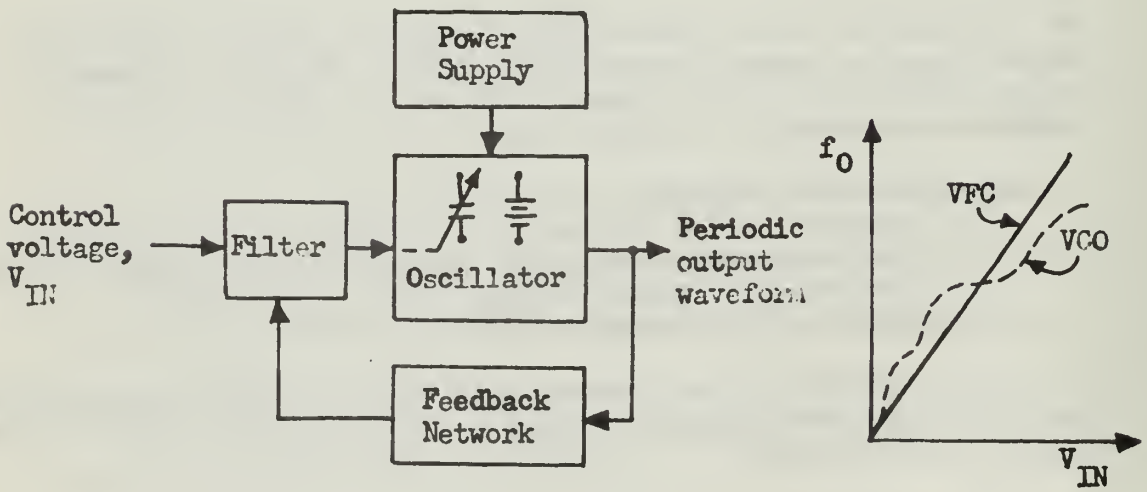
(d) The fundamental output frequency is f_{OSC}; K is typically positive and real; τ is some appropriate transit time for mobile charge carriers moving across a region.



(a). Block diagram of a basic oscillator.



(b). Controlled-parameter VCO.



(c). VFC.

Figure 2-3: Evolution of a VFC.

conditions of the oscillator, including its output frequency. This fact is indicated schematically by the capacitor and battery in Figure 2-3(a).

Oscillators are of course composed of active and passive components. Output frequency of any oscillator depends on the values of its passive components and references; typically, the only requirement placed on its active devices is some sort of minimum gain. In general, the oscillator configuration selected dictates the output waveform; "control" of an oscillator usually means controlling its output frequency.

There are three possibilities for a VCO: the applied voltage may be made to control one or more parameters, one or more references, or some combination of parameters and references in an oscillator. In all cases, there is some resulting voltage-frequency characteristic. Figure 2-3(b) shows a generalized controlled parameter VCO, with its transfer characteristic.

As mentioned earlier, a VFC consists of a VCO plus some extra circuitry, indicated by the ambiguous terms "filter" and "feedback network" in Figure 2-3(c). The purpose of the extra circuitry is to force an overall linear input voltage-output frequency relationship, as indicated in Figure 2-3(c).

Note that, in both the VCO and VFC, whatever furnishes the control voltage may also furnish energy, in addition to that provided by the power supply.

So far, nothing has been said about what may constitute oscillator, filter, or feedback network. It is tempting to rule out immediately any circuits which cannot be fabricated completely

(at least in theory) in monolithic form. For example, it might seem that configurations requiring large, high-Q inductance can be disregarded. Hachtel indicated which of the oscillator types of Table 2-1 were "integrable" (i.e., capable of being totally constructed in monolithic form). Not surprisingly, Hachtel concluded that the only integrable oscillators were those without inductance: oscillators using RC phase shift, junction transit time effects, or a combination of both.

In another instance, Howard and Pederson[10] investigated integrated VCO's, and stated that the only suitable candidates were circuits whose output frequencies are determined by resistors and capacitors. Howard and Pederson went on to conclude that, excluding gain control of active devices, integrated VCO's must be based on voltage-variable resistors or capacitors. This line of reasoning shows a dangerous lack of familiarity with the methods and economics of current monolithic IC's. As is pointed out in Appendix II, optimum economics may well dictate that a circuit consist of both an IC and external discrete components. Hence no VCO scheme can be rejected simply because all of its components cannot be built on a single chip. For this reason some of the VCO circuits considered in the next section are not completely "integrable".

CURRENT VCO/VFC METHODOLOGY

In this section we cover existing methods of realizing VCO's, and of combining VCO's and other circuitry to form VFC's. We will do this within the theoretical framework outlined in the preceding section.

The controlled parameter circuit is the more obvious type of VCO. Depending on the oscillator used, the controlled parameter might be resistance, inductance, capacitance, or a combination indicated by something like reactance or phase shift. Control can be either mechanical or electrical. Mechanical control could be accomplished by using a servomotor to vary the spacing between capacitor plates,[11] or to change inductance by moving a core inside a coil. On the other hand, there are eight devices which permit direct electronic control of at least one of the parameters of interest. Possibly the earliest such device is the reactance tube, which is discussed fully in the literature.[12] The varactor diode, which has recently become popular, provides a low, but voltage-variable capacitance.[13] Voltage-variable resistors are also available: currently one may choose among semiconductor diodes and both bipolar and field-effect transistors. Other methods exist which provide a measure of direct electronic control, but which have not achieved much acceptance: these comprise varying the inductance of an iron-core coil by introducing a DC signal,[14] controlling the phase shift (i.e., transit time) of a p-n junction,[15-16] and operating a transistor in its "inductive region".[17-18]

A controlled reference circuit is somewhat subtle. The output frequency of some oscillators depends not only on parameter values, but also on some reference current or voltage which may be appreciably varied. For instance, the frequency of the basic astable multivibrator may be varied over a wide range by changing a supply voltage.[19]

Similarly, the uni-junction transistor (UJT) relaxation oscillator[20] changes frequency as its bias current varies. The third common VCO in this category consists of an integrator and some type of switch. Here the integrator generates a ramp in one direction until its output voltage equals some reference voltage; then the switch changes the polarity of the voltage at the integrator input, causing the ramp to reverse direction. Both saw-tooth (integrator output) and square wave (switch output) waveforms are available in this circuit.

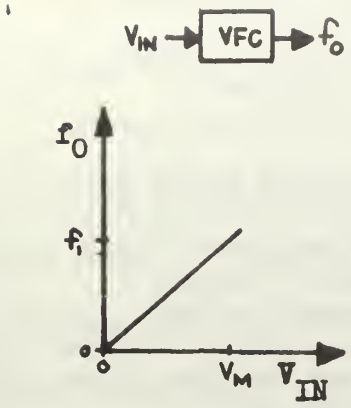
The short list above covers essentially every available VCO scheme. Clearly each possibility may be used to make a VCO from more than one oscillator in Table 2-1. For instance, a varactor (variable-capacitance) diode might be used in any of the seven oscillators in Table 2-1 which utilize type "E" (electric field) energy storage.

The VCO must be somehow transformed into a VFC; i.e., by definition, the VCO's voltage-to-frequency characteristic must be linearized. The ideal VFC characteristic is indicated in Figure 2-4(a). There are five usual alternatives:

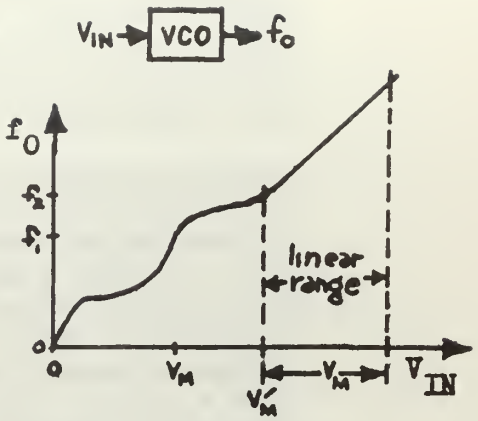
1. The VCO, Figure 2-4(b), might be accepted just as it is; some VCO's have voltage-to-frequency characteristics which are acceptably linear for some applications.

2. The VCO might have a "tractable" voltage-to-frequency nonlinearity; i.e., suitable "shaping" of the input voltage, before it is applied to the VCO, may result in a relatively linear over-all voltage-to-frequency characteristic, as shown in Figure 2-4(c).

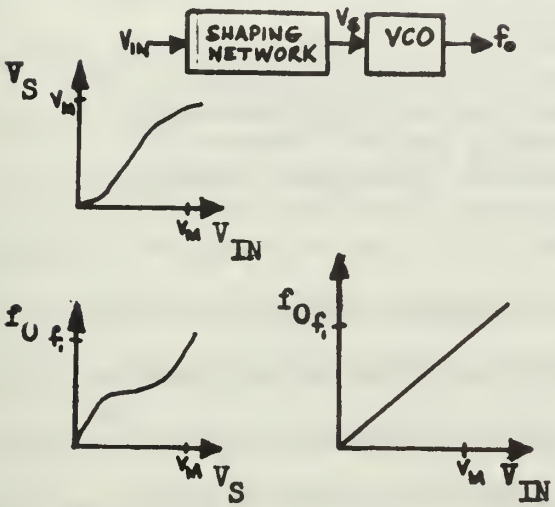
3. Negative voltage feedback could be employed (Figure 2-4(d)). The circuit shown here is essentially a nearly linear voltage-to-voltage device (i.e., an amplifier) when its output is considered to be the frequency-to-voltage



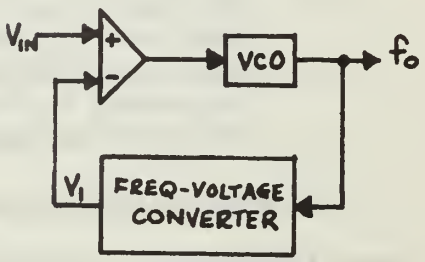
(a). The ideal VFC.



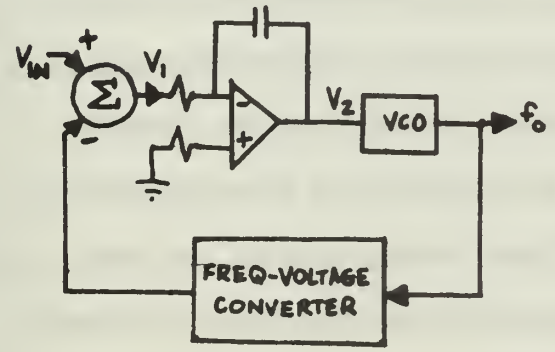
(b). The basic VCO.



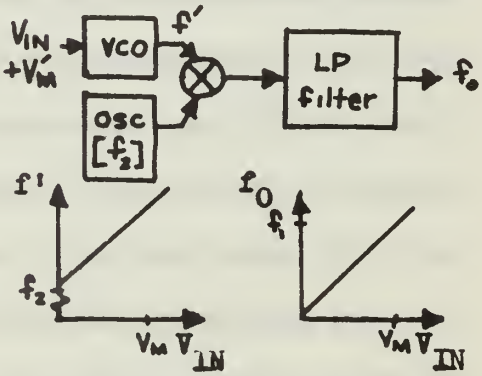
(c). Shaping.



(d). Negative-feedback system.



(e). Proportional-error system.



(f). Heterodyning system.

Figure 2-4: The ideal VFC and five practical approximations.

converter (low pass filter) output (V_1). Hence any negative voltage feedback decreases the gain but linearizes the V_{IN}/V_1 transfer function, which means that the V_{IN}/f_{OUT} transfer function is also made more linear.

4. Negative feedback could be used in a circuit analogous to the proportional-error control system. This circuit, illustrated in Figure 2-4(e), compares the input signal with a voltage proportional to the output frequency, and applies the error (V_1) to the integrator. The integrator's capacitor can be viewed as a memory element: it stores the VCO input voltage (V_2), and modifies it so that V_1 goes to zero. Note that virtually any VCO voltage-to-frequency characteristic is acceptable in this circuit, provided that it has a positive slope (i.e., an increase in input voltage magnitude causes an increase in output frequency).

5. The VCO might be linear over the desired bandwidth, but with the linear range centered at a relatively high frequency, so that heterodyning the VCO output with a stable oscillator will result in VFC output frequency components in the desired range. This last method is indicated in Figure 2-4(f).

We now consider a sampling of VCO papers published over the past two decades, to illustrate evolving techniques and enhance our perspective for viewing the various alternatives. Artzt,[21] in 1944, reported the successful operation of a tube RC phase-shift VCO; resistance (in this case, input resistance of a vacuum tube) was varied to achieve FM. Artzt reported that previous low frequency VFC's had used reactance tubes with heterodyne linearization. In 1949, Ames[22] described his design of a wide-range VCO; again the basic oscillator used RC phase shift, but "RC" in this case was actually provided by capacitively loaded cathode followers which gave a voltage-controllable phase shift. Also in 1949 was one of the earliest mentions of voltage control of the output frequency of an astable multivibrator: Sturtevant[23] described the general principles involved, and employed a voltage-controlled

constant current source to linearize the astable's voltage-to-frequency characteristic.

During the 1950's transistors came to popularity; Giacolletto[24] in 1957 described another RC phase-shift VCO, this time using transistors. Giacolletto was concerned with frequencies where the transistors provided a significant portion of the total phase-shift, so that FM was possible by varying transistor bias.

Of course, there was a continuing need for VFC's for applications which demanded wider frequency ranges and better linearity than a simple VCO could deliver. Two papers were published in 1961 which utilized the negative feedback VFC approach described earlier: Long[25] developed a rather complex VFC based around a Shockley 4-layer diode oscillator, which also included a monostable multivibrator and level shifting for output pulse forming, and used a differential amplifier for inserting the negative feedback into the forward path; Voeker[20] described a much simpler circuit which consisted essentially of just a unijunction transistor relaxation oscillator as the VCO, and again a differential amplifier.

Also in 1961 Greiner and Morgan[26] returned to the RC phase-shift VCO, using voltage-control of diodes' small signal resistance. The heterodyne VFC was still a serious choice for designers; in 1962, Bell and Chiunti[27] described an elaborate VFC which mixed the outputs of a 1.2-2.2 KHz VCO and a 1.2 KHz fixed oscillator, with filters and feedback to get a very linear 0-1.2 KHz VFC. In 1963, Biddlecomb[28] rediscovered the use of constant-current sources in a solid-state astable multivibrator; just as Sturtevant had noted

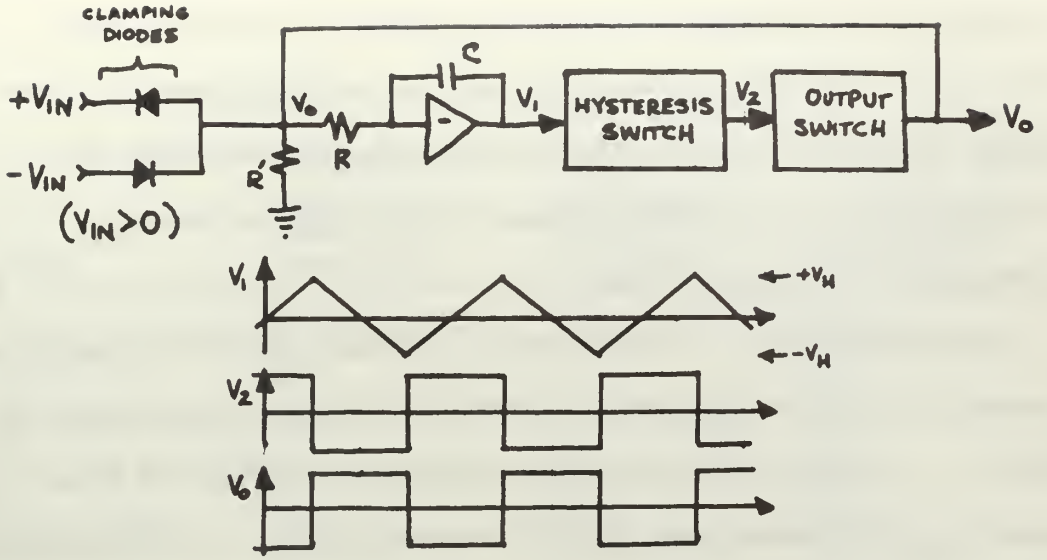
14 years earlier, Biddlecomb found that the result was a linear, wide-range VCO. Goodman[29] in 1964 conducted an extensive investigation of the bipolar-transistor astable multivibrator as a VCO, but he was primarily concerned with stability and linearity and was content with a 2:1 frequency range.

Integrated circuits were becoming accepted by this time, and circuit designers began to examine mechanisms which were suitable for integration. Uzunoglu[16] in 1966 mentioned the possibility of building a VCO using a semiconductor delay element as a voltage-controlled phase-shifter in a feedback path; a similar circuit was described by Yanai.[15]

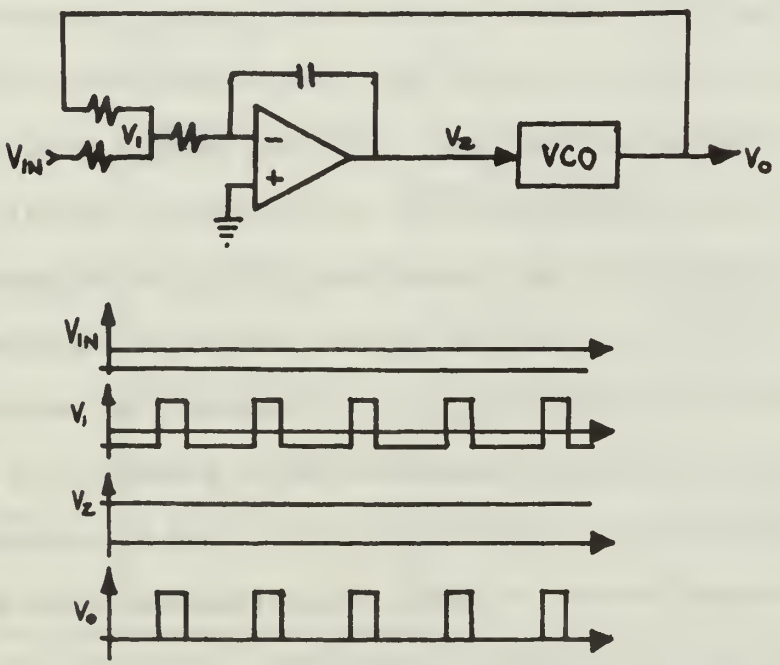
A final example of VCO design diversity is found in the 1967 paper by Giroux,[30] describing a circuit which used voltage-controlled diode resistance in a Wien-bridge oscillator.

Now that we have scanned some previous approaches to building VCO's and VFC's, it is interesting to pause here and examine some system details of two current VFC's: the Wavetek Model 104 Voltage Controlled Generator (VCG) and the Dymec Model DY-2210 Voltage-to-Frequency Converter. These serve to illustrate current VFC engineering practice, and provide intuitive insight into the VFC design problem.

The Wavetek Model 104[31] Figure 2-5(a), is an example of the VCO used directly as a VFC, with no additional linearizing circuitry. It consists essentially of the integrator-plus-switch VCO discussed earlier. The Model 104 must depend on precise, stable operation of each of its components to insure a low output error. The VCO output voltage (V_0) is also the integrator input voltage and determines



(a). Wavetek Voltage Controlled Generator (Model 104): basic block diagram and waveforms.



(b). Dymec Voltage-to-Frequency Converter (Model DY-2210): basic block diagram and waveforms.

Figure 2-5: Two contemporary VFC's.

the slope of the integrator output (V_1); when V_1 reaches a fixed value ($\pm V_H$), the hysteresis switch and output switch change states in turn, causing a change in V_O which reverses the polarity of the integration. Note that in Figure 2-5(a), $R' \gg R$, and V_{IN} is the positive applied voltage.

The Dymec DY-2210,[32] Figure 2-5(b), is built around a transistor blocking oscillator; i.e., an "IC negative-resistance oscillator" in Table 1-1. Control of the VCO here consists of varying the bias current of the blocking oscillator's transistor; this is the "variable-reference" control mentioned earlier. The DY-2210 uses the proportional-error linearization shown in Figure 2-4(d).

Table 2-2 compares these two configurations, which indicate what might be expected of general-purpose VFC's, with a representative VFC designed for industrial control use: the Acromag Model 1305-LX-1 Electronic Integrator Totalizer. This last device, in spite of its resounding title, is merely a VFC. Unfortunately, circuit details were not available for the Acromag Model 1305, but its specifications, listed in Table 2-2, illustrate typical industrial requirements.[33]

Referring to Table 2-2, note that apparently an industrial control VFC is similar to the general-purpose VFC's, especially in accuracy, temperature coefficient, power requirements, and physical size. The only notable differences are lower output frequencies and a surprisingly lower price for the industrial control VFC. The lower output frequencies are necessary in this case because the Acromag Model 1305-LX-1 is intended for use with a mechanical counter; they might be too low for accurate monitoring of some process variables.

Table 2-2

COMPARISON OF THREE CONTEMPORARY VFC'S

ITEM	Wavetek 104 Voltage-Controlled Generator	Dymec DY-2210 Voltage-to-Frequency Converter	Acromag 1305-LX-1 Electronic Integrator-Totalizer
Output frequency range (a)	.0015-100K Hz	0-10K Hz	0-3.33 Hz
Maximum output frequency change	20:1	(not listed)	20:1
Approximate accuracy (b)	0.1 per cent	0.1 per cent	0.1 per cent
Input voltage range	0-4.75 volts	0-1 volts	0-4 volts
Input impedance	10K ohms	1M ohms	20K ohms
Output impedance	50 or 600 ohms	3K ohms	(not listed)
VCO/VFC type	Integrator-plus-switch VCO	Proportional-error VFC with blocking oscillator VCO	(not listed)
Output frequency drift	(not listed)	0.02%/^{o}C, 10-50^{o}C	0.02%/^{o}D, 0-50^{o}C
Circuit	Solid state	Hybrid (tubes, solid state)	Solid state
Volume, weight, power requirements	286 cu.inches, 8 pounds, 5 watts	847 cu. inches, 20 pounds, 40 watts	264 cu.inches, 4 pounds, 10 watts
Price	$595	$895	$199

(a) Frequency range listed is absolute limits; maximum frequency change is for a given control setting.

(b) Accuracy is given in per cent of full-scale frequency.

Howard's and Pederson's previously mentioned paper[10] is the only one unearthed in a comprehensive literature search which specifically considers integrated VCO's. Because of this, their final design is worthy of examination. Howard and Pederson limited themselves to the RC phase-shift oscillator, with voltage-variable resistors or capacitors, for their VCO design. The varactor diode was considered as a voltage-variable capacitor; it was rejected because its capacitance was too low for the frequencies they required, and because it would require extra processing steps if it were part of a monolithic IC. Instead, field-effect transistors (FET's) were selected as variable resistors. The final circuit design included FET's, bipolar transistors, 58KΩ total resistance, and .02μf total capacitance. Since simultaneous production of both FET's and bipolar transistors is not currently feasible, and since monolithic area requirements for .02 μf compatible capacitance are prohibitively large, a production version of the Howard-Pederson VCO would probably be much like their breadboard model: resistors and bipolar transistors on one chip, FET's on another, and separate discrete capacitors. In short, their integrated VCO is not "integrable" by the same criteria that led to its design.

THE FINAL CHOICE

At this point we have considered applications, theory, and existing designs for the VFC. Economics must necessarily be the ultimate basis for decisions in engineering. In the initial stages of linear IC design, the high initial tooling costs and the expense of any changes in production circuits provide two essential economic criteria:

1. A very large potential market must exist;* and

2. The circuit design used must be nearly optimum from the standpoints of both cost and performance.

A large potential market does exist for an integrated VFC in the area of industrial controls. The discussion of VFC applications pointed this out and went on to illustrate other possible market areas. Now we are concerned with the second economic criterion: based on the pertinent theory and the lengthy discussion of present VCO's and VFC's, we must select the best possible circuit configuration.

In order to select a near-optimum functional configuration we must first define our design objectives; then narrow the field of possible choices by considering these objectives, practical engineering factors, and monolithic IC limitations; and finally choose among whatever alternatives remain.

We have previously noted that the industrial control requirement is the intended design objective for our integrated VFC, and that this requirement fits nicely with monolithic IC capabilities. Specifications for such an application are somewhat arbitrary, but the following are compatible with other typical elements of an automatic control system, and agree previously discussed factors;

INPUT VOLTAGE RANGE:	0 - 10 volts, DC
OUTPUT FREQUENCY RANGE:	0 - 1 KHz
OUTPUT WAVEFORM:	Constant-width pulse train
ACCURACY:	$\pm$ .1% of full-scale output frequency

Additionally, the following are typical of current volume-production monolithic IC's:

---

*As mentioned in the Introduction, minimum efficient production of linear IC's is about 100K circuits/year for each linear IC design produced.

PACKAGE:	Modified (12-lead) TO-5 can
POWER SUPPLIES:	+ 15 volts, - 15 volts, DC
DISSIPATION:	150 mw

The preceding section included three VCO approaches which are unsuitable, provided that other methods will give equivalent performance. First, mechanical parameter control may be dismissed: for similar performance, an electronic device is normally smaller, cheaper, and more reliable than a mechanical one. Second, we rule out inductors and transformers if at all possible; these are in general large, noisy, expensive, imprecise, and susceptible to stray magnetic fields, by comparison with other components.[34] And third, for obvious reasons, we discard the reactance tube. Note that ruling out inductance means disregarding the same oscillators as Hachtel did,[9] but for different reasons.

Monolithic IC limitations further restrict our selection. The pertinent IC design considerations at this point, condensed from Appendix II, are:

1. Most of the VFC circuit functions should be integrable; at the very least, all active devices and their biasing networks should be realizable on a single chip of moderate size (on the order of 65 mils by 65 mils, maximum). This is of course to take full advantage of the reliable, labor-free interconnections and the very inexpensive bipolar transistors afforded by standard (i.e., six-mask) IC's.

2. The VFC circuit to be integrated should be relatively insensitive to typical IC deficiencies, such as the lack of precision resistors, and should exploit the various advantages of IC's, such as V_{BE} matching.

The first consideration above means that FET's, four-layer diodes, and similar exotic devices should not be considered; and that VCO's and VFC's which depend on these devices (e.g., the Howard-Pederson varistor-FET VCO[10]) are then not suitable for our design.

There is one very stringent aspect of the rough specifications above which should be examined now: the requirement for wide frequency variation. Variable-parameter VCO's have output frequency relations in terms of the parameter magnitudes of passive devices, such as

$$f_o = K/RC$$

Clearly, achieving wide frequency variation by changing the magnitude of a single parameter, such as capacitance in the equation above, would be very awkward if not impossible. For this reason we will omit all variable-parameter VCO's from any further consideration.

One slightly subtle characteristic of all VFC's is their ultimate reference: somewhere in every VFC is some absolute quantity, such as resistance or voltage, which permits a form of measurement of the input voltage. Also, it is desirable to minimize the amount of application aggravation: as will be discussed in the next section, the IC designer tries to minimize the extra components and interconnections needed to use a given IC. Minimizing user aggravation would seem to require that the VFC reference be incorporated in the chip; this in turn means that a voltage reference is the most likely choice, since it is earily realized in an IC (by some kind of diode) and readily calibrated if fine adjustments are necessary.

It should be clear that the basic IC limitations preclude using an integrated VCO by itself as a VFC. Our wide frequency range and .1% accuracy requirements make an open loop, integrated VFC virtually impossible due to the inherent IC nonlinearities and chip-to-chip variations.

At this point we are ready to answer two questions:

1. What basic VCO should we use?

2. How shall we structure the VFC using this VCO?

We have already limited our VCO selection to a controlled-reference circuit, using only transistors, diodes, resistors, and capacitors; and we have recognized the need for some kind of linearization feedback to combine with the VCO in order to build our integrated VFC.

It is impossible to make any sort of "best" choice for either VCO or VFC. In neither case do we have a truly exhaustive list of circuits to insure that we even consider all possibilities. However, there is one VCO which does meet all of our requirements and is an obvious candidate: the voltage-controlled astable multivibrator. And for a VFC the proportional-error system is the most intuitively appealing, in that it provides continuous error correction.

The astable multivibrator in a proportional-error VFC is our final choice for the integrated VFC. While this may not be the best choice, it is nonetheless a good one. Figure 2-4(e) indicated the basic VFC arrangement, which included a frequency-to-voltage converter in the feedback loop, and the usual summing junction. Since we have constant-width, unipolar output pulses at a variable frequency, frequency-to-voltage conversion merely requires a low-pass filter. Also, the summing junction can be eliminated by applying the control voltage and the feedback (DC) signal to the same point in the forward path but at different polarities. And, finally, since the integrator is itself a low-pass filter, we can eliminate the separate low-pass filter from the feedback path.

Figure 2-6 shows the functional configuration we have selected, and some typical waveforms. Operation of this VFC is fairly straightforward: the integrator integrates the difference in the input signal (V_{IN}) and the DC component of the output signal (V_O), so that the integrator output (V_C) is at the correct value to make this difference zero. When the difference is zero, the output frequency (f_O) is directly proportional to V_{IN}, as required.

For instance, referring to Figure 2-6, consider the step response of the VFC. Initially V_C is just a ramp with slope proportional to V_{IN}. As long as V_C is below the turn-on voltage* of the astable, the astable output is at zero frequency (i.e., a constant zero volts). As mentioned before, the integrator essentially only sees the DC component ($\overline{V_O}$) of the astable output. The integrator output is actually the integral of $V_{IN} + \overline{V_O}$, but this is equal to the integral of V_{IN} before the astable turns on. When V_C reaches V_{C1}, the astable turns on. Now the astable output has a non-zero average ($\overline{V_O}$), so the magnitude of the integrator input ($V_{IN} + \overline{V_O}$) is reduced. This in turn reduces the slope of V_C. Steady state is reached when the astable output is at the desired frequency (f_O); here V_{IN} and $\overline{V_O}$ are equal in magnitude, so the integrator input is zero (V_{IN} is negative), and the integrator output stays constant at the value (V_{C2}) corresponding to f_O on the astable's voltage-to-frequency transfer characteristic.

---

*In general, a voltage-controlled astable multivibrator will have some minimum frequency of operation (excluding zero frequency). We use "turn-on voltage" to refer to the voltage corresponding to this minimum frequency (i.e., the voltage required for the astable to just turn on).

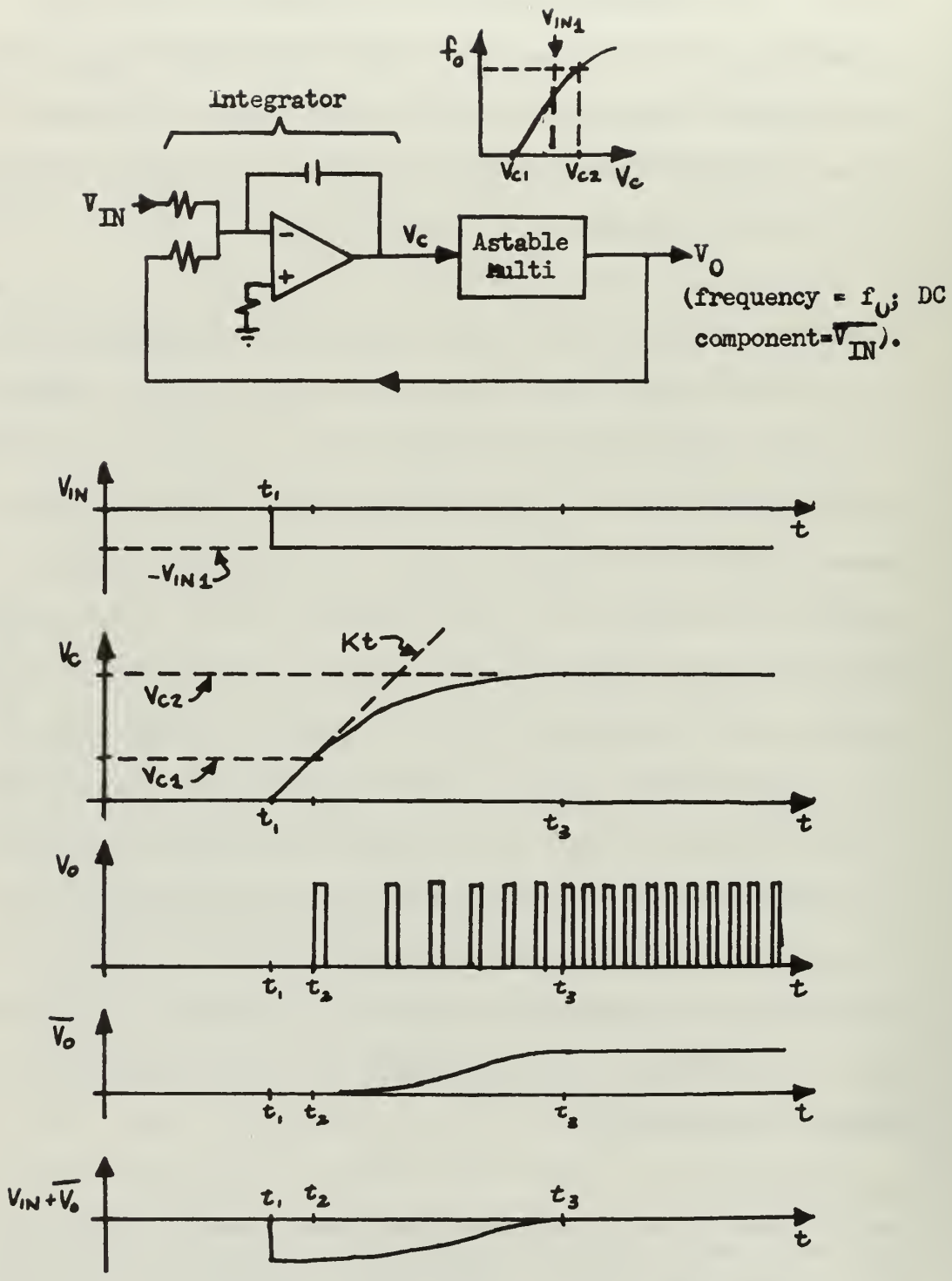


Figure 2-6: Functional configuration and waveforms for the integrated VFC.

The above explanation is of course oversimplified. The time scale in Figure 2-6 is distorted, and matters of timing, scaling, and whether or not steady state can be reached have been omitted, all in the interest of clarity. These will be more fully explained later. One important aspect of the circuit should be clear after a little study: the nature of the feedback and general arrangement is such that the astable must have a positive voltage-to-frequency characteristic (i.e., an increase in the magnitude of V_C, for $V_C > V_{C1}$, must correspond to an increase in f_O).

One final qualifier should be added to this entire circuit selection procedure: we have restricted ourselves to the capabilities of standard <u>production</u> monolithic IC's. As Lin and his colleagues pointed out in a recent state-of-the-IC-art survey,[35] monolithic devices, such as SCR's, are now feasible; certainly, in time, even more exotic devices may become part of standard production monolithic IC's.

3. CIRCUIT DESIGN

The development of an IC is outlined in the Introduction; as shown in Figure 1-2, the design phase of IC development, discussed in this section, is governed by design constraints forced by the IC technology, and design objectives provided in a set of circuit specifications.

IC development first involves a value judgement: it must be decided whether an IC satisfying the design objective seems feasible under the various technological constraints. In the preceding section we arrived at a functional configuration which appears amenable to monolithic integration. Of course, as Appendix II points out, total integration is never essential; instead, a combination of external discrete components and a monolithic IC is often the optimum solution to a set of design objectives. For instance, most monolithic IC linear amplifiers, regardless of their application, require external passive components for frequency compensation. In our design, based on the functional configuration in Figure 2-6, external components are necessary at least for the feedback capacitor in the integrator, and for cross-coupling capacitors in the astable multivibrator.

In this section we examine the evolution of the circuit design for our integrated VFC. First, we must define the degrees of freedom of the IC designer: we list monolithic IC design rules, which follow directly from the technological constraints discussed in Appendix II. Next, typical parameters of the components available for use in the monolithic IC are listed. And finally we develop the integrated VFC circuit design.

Before we consider its details, two aspects of the IC design process merit mention:

First, it is important to recognize that monolithic IC design is primarily an empirical process. Circuit complexity and capability exceed the limits of semiconductor and circuit theory in analysis and synthesis.[1] Typically a monolithic IC design is devised largely by intuition, and evaluated by breadboard testing. The design rules below reflect this empirical nature.

Second, monolithic IC design is predicated on the basis of a standard production line. The major monolithic IC manufacturers have found that the most profitable mass production occurs when all circuits are produced in exactly the same steps, differing only in masks[2]; this standard production has given each IC manufacturer much detailed information on the components from his production line, so that a list of component parameters (such as the typical one in this section) is a common tool of the IC designer.[3]

THE MONOLITHIC IC DESIGN RULES

Based on the limitations and capabilities of monolithic IC fabrication, a set of design rules has become widely acknowledged.*

---

*The information on IC design rules and component parameters is a condensation and correlation of numerous IC design papers.[4-25] The Introduction stressed the fact that monolithic IC capabilities and constraints were similar to those of IC's from other technologies; it is interesting to note the close similarity between the monolithic (bipolar) IC design rules listed here and the constraints given for designing monolithic MOS IC's[26] and multichip hybrid IC's.[27]

These rules identify certain components or arrangements with cost labels (e.g., "expensive"); Appendix II shows that the cost of a component is directly related to the chip area it requires; cost and area are usually synonymous. The rules are:

a. Resistors. Use small values of resistance; resistance is expensive. If a 60 mils square chip contained only a single base-diffusion, .5 mil wide resistor, it would have a value of only about 1.5MΩ; a practical upper limit for total resistance of an IC's diffused resistors is 150KΩ.

Make circuit performance, including operating points, dependent on resistor ratios rather than resistor absolute values.

b. Capacitors. Use small values of capacitance, or better yet, use no capacitance; capacitance is very expensive. If an entire 60 mils square chip was processed as a single MOS compatible capacitor, it would have a value of only about .001μf.

c. Inductors. Use no inductance; inductors are impossible to integrate in monolithic form.

d. Diodes. Use suitably connected npn transistors for all diodes, including Zener diodes. The B-E junction diode, with C-B junction shorted (Figure II-6(a)), is preferable wherever its low breakdown voltage is acceptable.

e. Transistors. Use npn transistors wherever possible; these are inexpensive and perform as well as discrete transistors; as opposed to pnp transistors which are inexpensive but perform poorly (lower h_{FE}, bandwidth). Make circuit performance depend on transistor parameter ratios (i.e., transistor matching) rather than absolute

values. As with resistors, transistor parameters have better ratio tolerances than absolute value tolerances. Exceptional matching is possible with V_{BE}.

f. External connections (IC package pins). Use the minimum number possible; these are expensive, both because of the large aluminum pads needed on the chip, and because of the labor costs in wiring the pad on the chip to the package lead. Also, the package to be used determines the maximum number of leads available; twelve leads are the most that can be accommodated by the popular modified TO-5 can.

g. Isolation regions. Although actual mask design follows both circuit design and breadboard evaluation, one aspect of the actual physical layout of the chip should be considered during circuit design: the number of separate isolation regions (regions surrounded by a single p+ isolation diffusion). These should be minimized since they are expensive; moreover, minimizing the number of isolation regions decreases parasitic capacitance in the IC.

h. Power requirements. Use low voltage supplies, preferably at typical IC values (such as +6V, -6V; +15V, -15V; +9V, -8V), to minimize power dissipation. The high component density of monolithic IC's requires that each component be operated at a very low DC power level. The package thermal resistance determines total permissable power dissipation. Voltage levels are limited by component ratings (usually transistor L^{V}_{CEO}).

i. Temperature stability. IC's can be made which depend on very close thermal tracking for temperature stability, since all components in an IC are very close together on a common substrate, and thus tend to be very close to the same temperature; very tight thermal tracking can be attained in adjacent components on the chip.

j. Adjustments. No component adjustments during production of monolithic IC's are feasible. This means that an IC design must function over the full range of expected parameter variations.

k. IC application. The amount of external components and interconnections required to achieve a desired circuit function with an IC should be minimized, since these tend to reduce the reasons (cost, reliability, size, etc.) for using the IC, and thus tend to reduce the IC's sales potential. Quite obviously, the object of IC design is to select circuits which exploit the inherent advantages of monolithic components, while avoiding configurations that are expensive or impossible to achieve in monolithic form. Often this involves functional substitution, such as the common approach of using a constant current source (active devices and small resistance) in an IC, in place of a large resistor.

MONOLITHIC IC COMPONENTS

Table 3-1 lists typical parameters for monolithic IC components.

It is noted above that an IC designer normally has detailed component information, based on a large data base from a standard production line. This information is usually proprietary, since it includes process and geometry details for realizing desired device

characteristics. No such information was available for this report, so we use the typical values of Table 3-1 for our IC design.

Very complicated IC models have been advocated for monolithic IC components, to account for their parasitic effects.[28] These models have ranged from distributed networks[29] to networks which include lumped equivalent elements for the parasitic effects.[30] Table 3-1 includes none of these parasitic effects, in any form; we use a much simpler model for our IC design.

This simplification is made for two reasons:

First, the primary purpose of any model must always be to facilitate design by providing a simplified symbolization of physical processes;[31] the complicated IC models mentioned above, which include parasitic effects, are too cumbersome to be readily manipulated. Unfortunately, theory has not been able to keep up with the empirical progress in IC design, to the extent that precise theoretical evaluation of current IC's is virtually impossible.[32]

Second, the parasitic effects which lead to model complications are often negligible for a properly designed monolithic IC, operated at relatively low ($<$ 1MHz) frequencies. Experience has shown that device intercoupling in monolithic IC's is usually insignificant.[33] For collector currents above 250 μa, collector-to-substrate leakage currents are similarly insignificant.[34] Isolation requires that the various collect-substrate junctions be reverse biased, but this is easily done by connecting the substrate to the most negative potential in the IC.

Table 3-1

TYPICAL MONOLITHIC IC PARAMETER VALUES

Symbol	Parameter	Value	Notes[a]
1. RESISTANCE			
$LV_{RR'}$	Limiting voltage across resistor	30 v	
LV_{RS}	Limiting voltage, resistor to substrate	30 v	
P_{MAX}	Maximum power dissipation	0.1 w	
-	Absolute value tolerance	$\pm$ 20%	(b)
-	Ratio tolerance	$\pm$ 4%	(c)
TCR	Temperature coefficient of resistance	+.2%/^{o}C; $\pm$.01%/^{o}C	(d)
2. HIGH SPEED DIODE (Figure II-6(a))			
V_F	Forward voltage	0.70 v	(e)
MV_F	Forward voltage match	$\pm$ 5 mv	
BV_R	Reverse breakdown voltage	6.5 v	
τ_R	Recovery time	< 5 nsec	
3. MEDIUM SPEED DIODE (Figure II-6))			
V_F	Forward voltage	0.72 v	(e)
MV_F	Forward voltage match	$\pm$ 8 mv	
BV_R	Reverse breakdown voltage	> 30 v	
τ_R	Recovery time	< 10 nsec	
4. npn TRANSISTOR			
h_{FE}	DC current gain, $\lvert I_C/I_B \rvert$	50	
LV_{CEO}	Limiting voltage, collector-to-emitter, base open	>30 v	

Table 3-1 (Cont.)

Symbol	Parameter	Value	Notes
f_T	Current gain - bandwidth	500 MHz	
C_{CS}	Collector-to-substrate capacitance	3 pf	
$V_{CE(sat)}$	Collector-to-emitter saturation voltage	0.01 v	(e)
$V_{BE(sat)}$	Base-to-emitter saturation voltage	0.8 v	
Mh_{FE}	h_{FE} match	$\pm$ 10%	
MV_{BE}	Base-to-emitter voltage match	$\pm$ 10 mv	
-	Drift of V_{BE}	-2 mv/^{o}C	(f),(g)
BV_{BE}	Base-to-emitter breakdown voltage (reverse bias)	6.5 v	
-	Drift of BV_{BE}	+ 1 mv/^{o}C	(g)
-	Drift of V_{BE} match (i.e., tracking)	$\pm$ 10μv/^{o}C	(g)
$TCV_{CE(sat)}$	Temperature coefficient of base-to-emitter saturation voltage	+ .2%/^{o}C	
BV_{CS}	Substrate-to-collector breakdown voltage (reverse bias)	80 v	
5. LATERAL pnp TRANSISTOR (h)			
h_{FE}	DC current gain, I_C/I_B	2	
6. VERTICAL pnp TRANSISTOR (h)			
h_{FE}	DC current gain, I_C/I_B	20	
7. TO-5 PACKAGE			
R_T'	Thermal resistance, case-to-circuit	50^{o}C/w	
R_T	Thermal resistance, free air-to-circuit	170^{o}C/w	

(a) T is ambient temperature; all T = 25^{o}C unless otherwise noted.
(b) R < 30K. (c) Ratio < 10:1.
(d) 0^{o}C $\leq$ T $\leq$ 125^{o}C and -55^{o}C $\leq$ T $\leq$ 0^{o}C, respectively.
(e) I = 1 ma.
(f) Drift refers to a definite change (as, mv), as opposed to temperature coefficient, a percentage change.
(g) -55^{o}C $\leq$ T $\leq$ 125^{o}C.
(h) Parameters for both types of pnp transistor are the same as for the npn transistor, with the exception of h_{FE}.

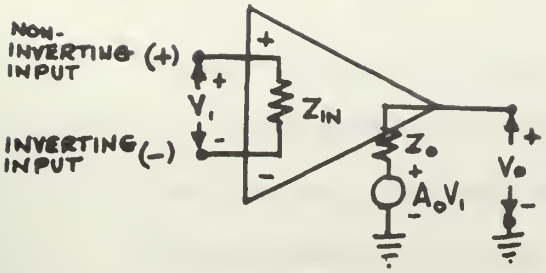
The most noticeable effect of IC parasitics is degradation of amplifier frequency response. Rather than attempt to analyze this complex phenomenon, we use rough assumptions to determine frequency response (and compensation requirements) in the IC design.[35]

INTEGRATED VFC DESIGN

In the following discussion we develop the circuit design for the integrated VFC. As shown in Figure 2-6, we require two major components for our VFC: an operational amplifier and an astable multivibrator. We first consider the operational amplifier: its general characteristics, its typical monolithic elements, and its design in the integrated VFC. Next, we consider the astable multivibrator: its classic form, and modifications to make it amenable to integration. Finally, we combine both major components into the integrated VFC design.

In designing these components we are restricted by the stringent design rules and a limited selection of components, both listed above. The monolithic IC designer has only two degrees of freedom: ingenuity in creating unique circuits, and optimization of component geometries.[36] We concentrate on the former, since the latter only serves to enhance performance of a working design.

The operational amplifier portion of the integrated VFC is a straightforward design problem; more than fifty different monolithic IC operational amplifiers are presently on the market.[37] The ideal operational amplifier, indicated in Figure 3-1(a), has infinite bandwidth, infinite voltage gain (A_o), and zero offset (i.e., $V_1 = 0$ when $V_o = 0$, and vice versa). Figure 3-1(a) indicates a differential-input operational amplifier: a positive voltage applied to the



$A_O = \infty$

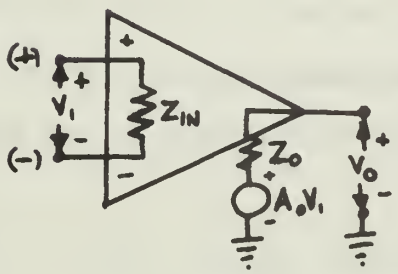
$Z_{IN} = \infty$

$Z_O = 0$

$f_T = \infty$

$V_O = 0$ when $V_1 = 0$

(a). Ideal operational amplifier.



$A_O = 10^4$ (80 db)

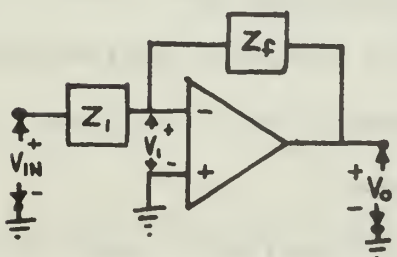
$Z_{IN} = 10K$

$Z_O = 50$

$f_T = 1MHz$

$V_O = 0$ when $V_1 = 5mv$ (offset)

(b). Typical IC operational amplifier.



For ideal operational amplifier...

$$-A = \frac{V_O}{V_{IN}} = \frac{Z_f}{Z_1}$$

(c). Inverting amplifier configuration.

Figure 3-1: The operational amplifier.

non-inverting input (marked with a plus sign) results in a positive output voltage, while a positive voltage applied to the inverting input (marked with a minus sign) results in a negative output voltage. An IC operational amplifier is of course limited to finite, non-zero input and output impedances, bandwidth, voltage gain, and offset; some typical IC operational amplifier parameters are indicated in Figure 3-1(b).[38]

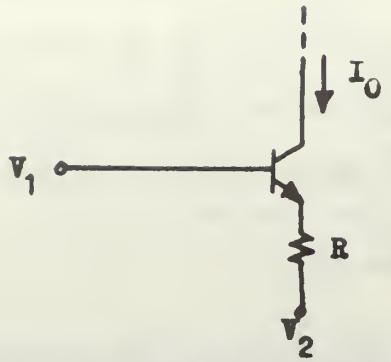
The properties of the ideal operational amplifier are valuable because when an ideal operational amplifier is used in a circuit with negative feedback, the performance of the circuit depends only on the feedback elements. For instance, an ideal operational amplifier in the simple inverting amplifier circuit of Figure 3-1(c) has an overall gain ($A = V_o/V_{IN}$) equal to the ratio of the feedback and input impedances:

$$|A| = \frac{Z_f}{Z_{IN}}$$

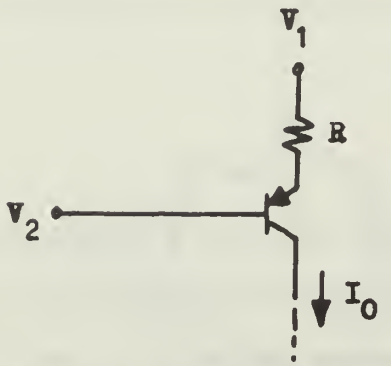
The analysis leading to the above expression, and other theoretical facets of operational amplifier applications, are widely covered in the literature;[39-45] these are not discussed here. Also, it has been shown that non-ideal operational amplifiers perform quite close to the ideal case: the parameters listed in Figure 3-1(b) are satisfactory in many applications.[45]

Three common building blocks for monolithic linear IC's merit detailed mention; these are the constant current source, the differential amplifier, and the level-shifting stage:

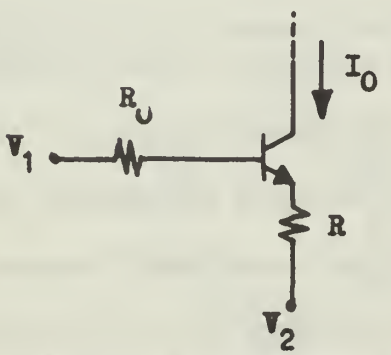
(1) The constant current source is shown in Figure 3-2 for both the npn and pnp transistor; note that the pnp current source is just the inverse of the npn current source, and that the npn



(a). The npn constant current source.



(b). The pnp constant current source.



(c). A modified npn constant current source.

Figure 3-2: The constant current source.

current source is more correctly a current "sink" since the actual direction of the controlled current (I_o) is into the circuit. In both of the basic current source circuits, for proper selection of V_1 and V_2 and under the usual assumptions (large h_{FE}, V_{BE} = .6V),

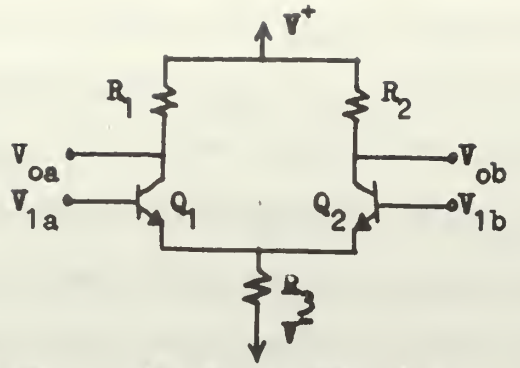
$$I_o = \frac{V_1 - V_2 - .6v}{R}$$

Figure 3-2(c) illustrates a modification of the basic npn current source; here, for proper selection of V_1 and V_2 and under the usual assumptions, the controlled current is independent of V_1, V_2, and R_0:

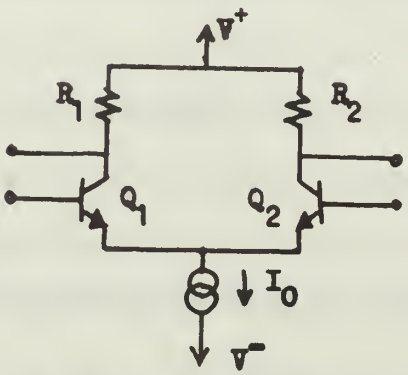
$$I_o = \frac{.6v}{R}$$

Clearly the constant current source is a valuable item for the IC designer, since it provides a large (theoretically infinite) resistance using active devices and small values of resistance: a large chip area effect is realized by a combination of small-area elements.

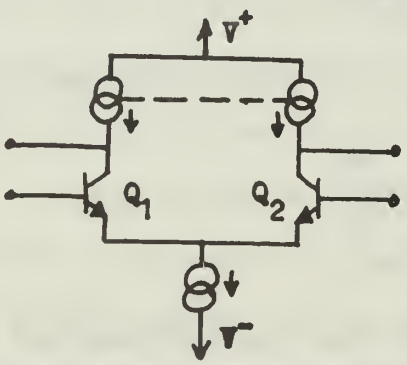
(2) The differential amplifier, shown in Figure 3-3, is another popular device in IC designs, because it takes advantage of the excellent transistor matching possible in IC's,usually requires a minimum of external capacitance compared to other configurations, and can be constructed so that its gain is dependent on resistor ratios and so that large resistance values are not required.[47,48] The differential amplifier is extensively analyzed in the literature;[49,50] this discussion is restricted to a few simple results and implications of such analysis. In the basic circuit (the "long-tailed pair"), Figure 3-3(a), a



(a). The basic differential amplifier.



(b). Addition of one constant current source.



(c). Addition of three constant current sources.

Figure 3-3: Evolution of an IC differential amplifier stage.

differential input signal ($V_{ia} - V_{ib}$) causes an amplified differential output signal ($V_{oa} - V_{ob}$); such a differential signal is commonly called a differential mode, or DM, signal.

In any real circuit, unbalances will exist; clearly we wish to amplify the DM signal more than any voltage common to both input terminals (called the common mode, or CM, signal). Middlebrook shows that one way of increasing the ratio of DM gain to CM gain is to make R_3 in Figure 3-3(a) very large, by replacing it with the constant current source as shown in Figure 3-3(b).[51] Here the constant current source symbol represents the npn circuit of Figure 3-3(a).

For the circuit in Figure 3-3(b), it has been shown[52] that, if

$$R_1 = R_2 = R$$

then DM gain is, under the usual approximations (small signal, large h_{FE}),

$$A_{DM} = \frac{R\, I_o\,(ma)}{52}$$

Also, again using the usual approximations, the input impedance is

$$R_{IN} = \frac{26\ h_{FE}}{I_o\,(ma)}$$

where R_{IN} is in ohms.[53]

Clearly we would like a high DM gain and a high R_{IN}, and the only way to achieve both is to make R very large. Here is another application for the constant current source: with constant current sources replacing all the resistors in the basic differential amplifier of Figure 3-3(a), we have the circuit of Figure 3-3(c), which has theoretically infinite gain and CM rejection (i.e., A_{DM}/A_{CM}), and potentially very high input impedance. The

collector-lead constant current sources in Figure 3-3(c) can be realized by the pnp circuits of Figure 3-2(b); the dotted line indicates "slaved" current sources: current sources with the same base voltage.

(3) Level shifting is necessary in DC-coupled amplifiers when successive amplification by npn stages is performed, since each successive amplification increases the DC component in its output: in effect, a growing, positive DC error is added to the signal. In order to have both amplifier input and output nominally at ground potential when no signal is applied, the amplifier must have a negative shift in DC level at some signal point within the amplifier; this level shift is usually accomplished by a Zener diode, by the combination of a constant current source and a resistor, or by a pnp transistor stage.

A study of current monolithic operational amplifiers shows that the typical design consists of four stages: a differential input stage, a second gain stage providing single-ended (unbalanced) output for a balanced input signal, a level shift stage, and an output stage; the output stage determines the output voltage and current limits, while the input stage provides most of the voltage gain. Flexibility is a major design objective of monolithic operational amplifiers: they must be suitable for use in a large variety of feedback configurations, and so they usually require several possible frequency compensation variations and stable operation for all anticipated applications.

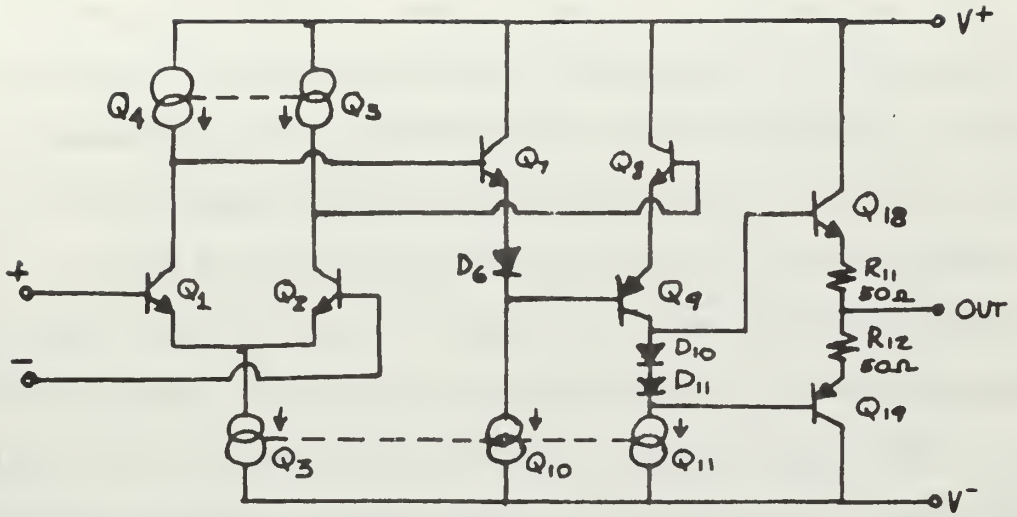
The operational amplifier in our integrated VFC has only one application: it is the basic element in an integrator. This single application means that the design can be cruder than the typical monolithic operational amplifier design; this also means that a single frequency compensation method is satisfactory.

The basic operational amplifier design for the VFC is shown in Figure 3-4(a); it consists of a differential input stage (Q_1,Q_2), a pair of emitter followers (Q_7,Q_8), a differentially-driven transistor (Q_9), and a classic complimentary push-pull output stage (Q_{18},Q_{19}).* The input stage uses the three current source (Q_3,Q_4,Q_5) configuration developed in Figure 3-3. The emitter-followers provide isolation to prevent succeeding stages from loading the input stage unduly. The differentially-driven transistor converts the double-ended output signal from the first stage into a single-ended signal to drive the output stage. The output stage is essentially a pair of emitter-followers, connected such that only one transistor (Q_{18} or Q_{19}) is conducting at a time. Diode D_6 and the constant current sources Q_{10} and Q_{11} provide bias control, while diodes D_{10} and D_{11} and resistors R_{11} and R_{12} reduce cross-over distortion in the output stage.

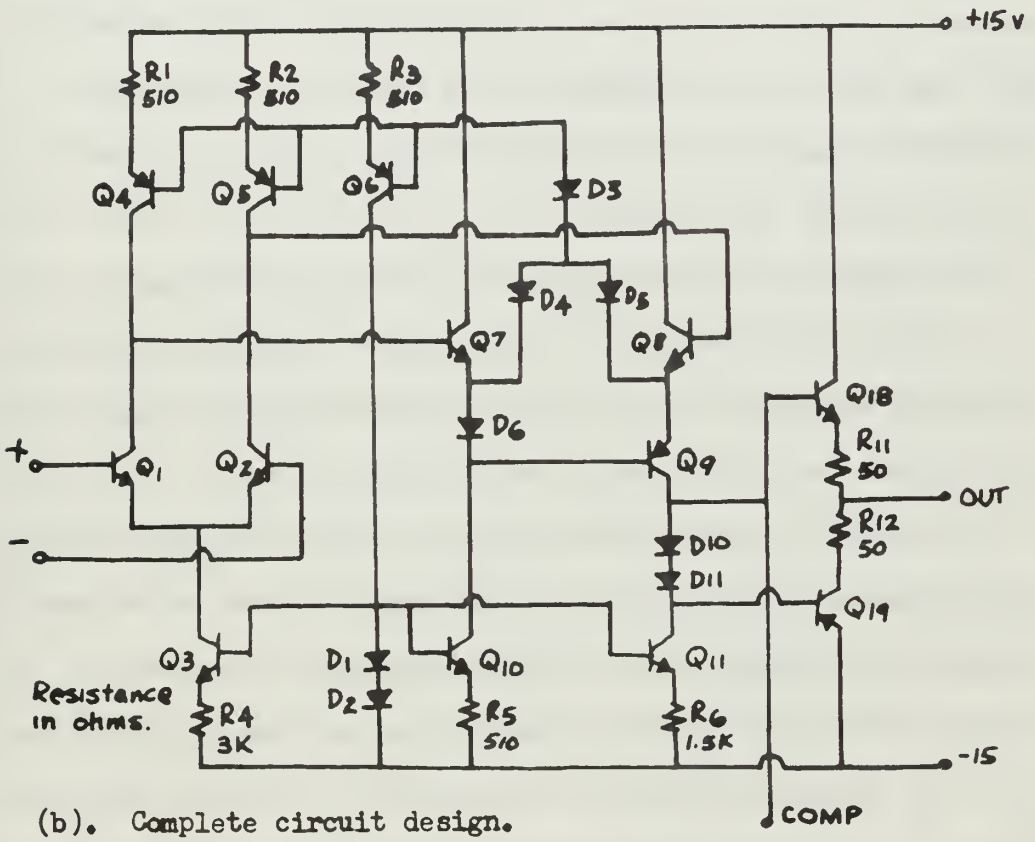
To illustrate the operation of the basic circuit in Figure 3-4(a), consider that the non-inverting (+) terminal is grounded, and a positive DC signal is applied to the inverting (-) terminal. Assume

---

*This portion of the integrated VFC design was developed by M. J. Cochran, Cintra Data Systems, Mountain View, California.



(a). Simplified circuit design.



(b). Complete circuit design.

Figure 3-4: The integrated VFC's operational amplifier.

that the Q_4 and Q_5 current sources act as large resistors, and that the Q_3 current source acts as an ideal constant current source. The signal causes an increase in I_{C2}; because the total current through the Q_1 - Q_2 pair is held constant by Q_3, the increase in I_{C2} is accompanied by a decrease in I_{C1}. This means that V_{C2} decreases (becomes less positive), and V_{C1} increases. The emitters of Q_7 and Q_8 follow this voltage change: V_{E7} increases, and V_{E8} decreases. Diode D_6 appears as a small incremental resistance to the signal, so V_{B9} increases. Both the increase in V_{B9} and the decrease in V_{E9} cause a decrease in V_{C9}. Both Q_{18} and Q_{19} operate as emitter followers, so the output voltage decreases also; if a load had been connected to the output, Q_{19} would have turned on to draw the necessary current. Note that the original positive signal at the inverting input terminal has resulted in an amplified, negative signal at the output terminal, as expected.

Note also that the design in Figure 3-4(a) represents a minimal operational amplifier configuration: it consists only of one differential stage, buffering, double-ended to single-ended signal conversion, and an output stage.

The complete circuit design, Figure 3-4(b), adds essentially only increased CM rejection to the minimal amplifier of Figure 3-4(a). An additional current source (Q_6) is necessary, of course, to control the bias of the slaved npn current sources (Q_3, Q_{10}, and Q_{11}). Q_6 controls the current through diodes D1 and D2, and thus controls the voltage across them; this is identical with the

configuration shown in Figure 3-2(c). It is the method of biasing the slaved pnp current sources (Q_4, Q_5, and Q_6) which provides the DM rejection: massive negative CM feedback is achieved by diodes D_3, D_4, and D_5.

If the circuit is operating normally, and no signal is applied, the slaved pnp bases are approximately one "diode drop" (.6V) above the equal collector voltages V_{C1} and V_{C2}.

If a DM signal is applied, the collector voltages V_{C1} and V_{C2} shift an equal but opposite amount. These voltages changes result in equal but opposite changes in the diode currents I_{D4} and I_{D5}, so that the total bias current through D_3 (I_{D3}) remains constant and the pnp current sources (Q_4, Q_5, and Q_6) remain near their quiescent operating points.

If, instead, a CM signal is applied, both I_{D4} and I_{D5} either increase or decrease in the same amount, so that I_{D3} changes also; this results in the negative CM feedback effect. For instance, assume that both V_{C1} and V_{C2} increase, so that V_{E7} and V_{E8} increase. Then I_{D4} and I_{D5} decrease, causing a decrease in I_{D3}. This decreases the operating currents of the pnp current sources; the decrease in I_{D4} and I_{C5} causes an effective decrease in V_{C1} and V_{C2}, so that the original CM effect is reduced. Similarly, the reduction in the operating current of Q_6 decreases the magnitude of the voltage drop across D_1 and D_2, which decreases the operating current of Q_3; this also reduces V_{C1} and V_{C2}, thus reducing the original CM effect. In other words, the diodes D_3, D_4, and D_5 produce negative CM feedback as previously stated.

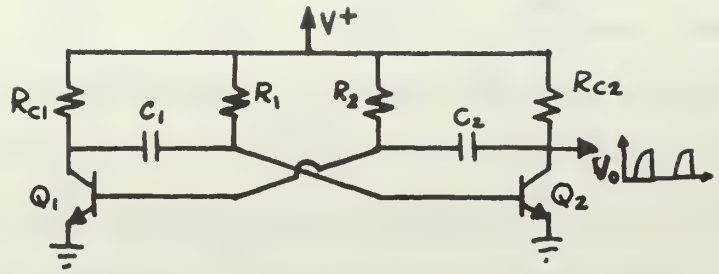
A frequency compensation terminal at the collector of Q_9 is shown in Figure 3-4(b); its use is explained in the next section.

Figure 3-4(b) indicates +15V and -15V power supply requirements: these values were chosen to permit wide output voltage variation; any smaller output-variation will then have smaller distortion than with smaller supply voltages.

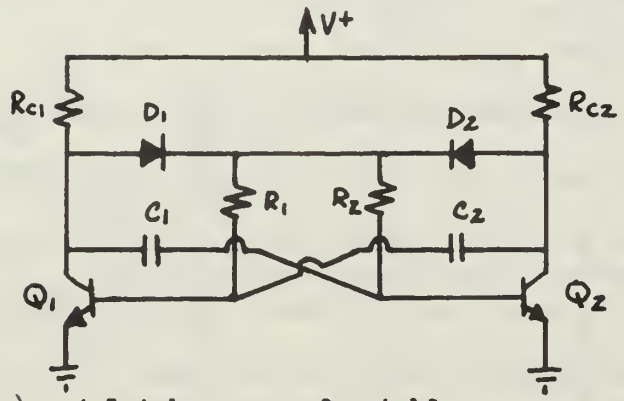
The astable multivibrator portion of the integrated VFC provides a different design problem than that for the operational amplifier: instead of simplifying an existing monolithic IC design, as with the above operational amplifier design, we must convert the common discrete astable circuit to a form suitable for integration. The classic astable is shown in Figure 3-5(a); this circuit is essentially unchanged from the one first reported by Abraham and Bloch in 1919.[54] Astable operation, which is widely explained elsewhere,[55] has three major drawbacks:

1. Since both transistors are biased for what would be saturation in the absence of the cross coupling capacitors, it is possible (and not uncommon) for both transistors to become simultaneously saturated when power is applied, or when some parameter is changed. This condition is called "latch-up"; a latched-up astable is inoperative.

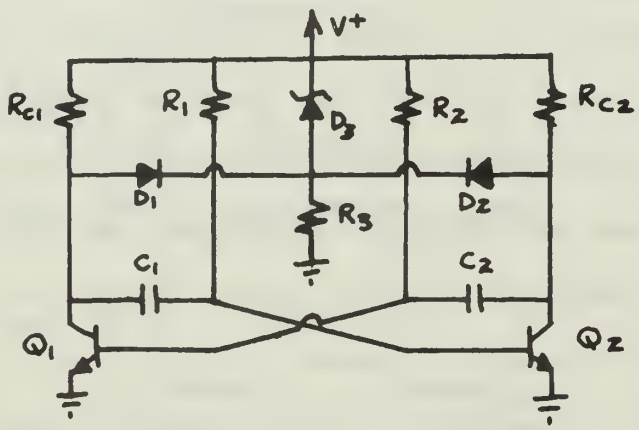
2. The transistion from saturation to cut-off requires capacitor charging at the collector node with a time constant CR_c; this leads to the characteristic rounded edge of the output waveform, shown in Figure 3-2(a), and what may be an unsatisfactorily long output waveform risetime.



(a). The classic circuit.



(b). A latch-up proof astable.



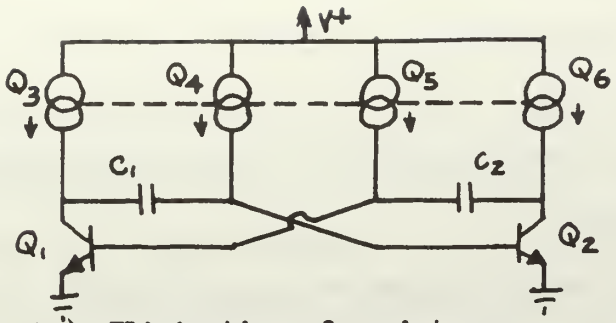
(c). An astable with catching diodes.

Figure 3-5: Common Astable Multivibrator Permutations.

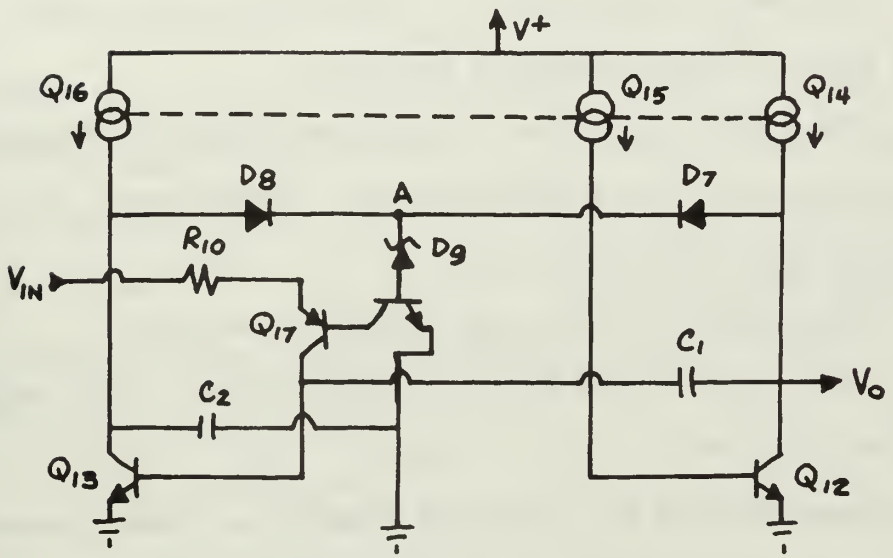
3. Drift in output parameters (especially frequency) may be excessive due to temperature, power-supply voltage, and component parameter variations.

Methods exist for remedying all three drawbacks. One common circuit for eliminating latch-up is shown in Figure 3-5(b); elementary analysis shows that this circuit cannot have both Q_1 and Q_2 simultaneously in saturation.[56] Perhaps the simplest method of decreasing rise-time is to clamp the collector of the cut-off transistor to a voltage less than the supply voltage, by what is called a "catching" diode; Figure 3-5(c) (after Goodman[57]) illustrates one method of using catching diodes. And, finally, Marcus and Smith have demonstrated that frequency stability can be significantly improved in an astable by using additional circuitry; for instance, with one circuit Marcus and Smith reduced frequency drift to less than 0.1 per cent for temperatures from -55° to $+75^{\circ}$C.

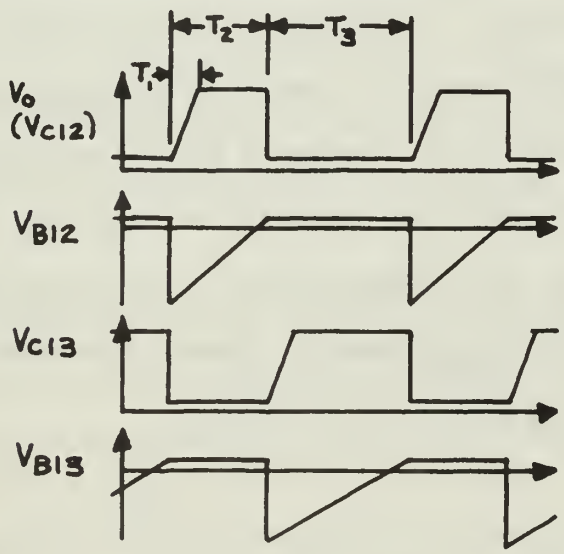
The immediate problem in adapting the classic astable circuit for monolithic integration is the need for large resistors: keeping collector current in the saturated transistor at 1 ma would require a 15KΩ collector resistor for the +15V supply decided on above, and this in turn would require base resistors on the order of 150KΩ. Substituting slaved current sources for the resistors in the classic circuit, as shown in Figure 3-6(a), makes the basic circuit integrable. The cross-coupling capacitors, C_1 and C_2, must be external components, as discussed above. Current sources have another advantage, in addition to requiring less chip area, over large resistors: base waveforms are linear rather than



(a). Elimination of resistors.



(b). Final circuit design.



(c). Waveforms for final circuit.

Figure 3-6: The integrated VFC's astable multivibrator.

exponential during the capacitor-charging interval, so the time when base voltage reaches the transistor turn-on voltage is more tightly controlled, which means that operation is more stable, especially at low frequencies (i.e., long charging times for the capacitors).

In addition to eliminating large resistors, there are four requirements for our monolithic astable:

1. The circuit should have a constant-width pulse train output, with a voltage-controlled frequency.

2. The circuit should have a positive voltage-to-frequency characteristic (i.e., an increase in input voltage causes an increase in output frequency).

3. The circuit should not be subject to latch-up.

4. The circuit should employ catching diodes to limit effective output rise time.

An examination of the literature revealed no single circuit design which satisfied all of the above requirements without prohibitive complexity. Satisfactory astable design must instead rely on the primary degree of freedom of the monolithic IC designer: ingenuity in the design of unique circuits.

Figure 3-6(b) shows the essential elements of the unique astable design for the integrated VFC;* this design meets all of the above astable requirements. Normal operation of the circuit in Figure 3-6(b) is as follows:

Assume that the circuit is biased properly, with a sufficiently positive input voltage (V_{IN}) for the astable to

*Patent applied for, docketed under Navy Case Number 48,014.

function. Assume also that initially Q_{12} is on (i.e., in saturation) and Q_{13} is off, at a point in time corresponding to the origin of the waveform plots, Figure 3-6(c). Q_{17} is a lateral pnp transistor, D_9 is a high speed diode, and D_7 and D_8 are medium speed diodes; nominal diode and transistor parameters are as listed in Table 3-1. With Q_{12} on, the current out of Q_{14} goes through Q_{12} and V_{C12} is about .01 V; V_{BE12} is about .8V. Q_{13} is off, so essentially all of the current out of Q_{16} goes through D_8, D_9, and Q_{20} to ground; Q_{20} is saturated and D_9 is broken down, so V_A is at about 6.3V and V_{C13} is at about 7.3V. Q_{17} is in the active region, with V_{BE17} at about 0.6V. With its low gain ($h_{FE} = 1$), Q_{17} acts like a "current splitter": I_{B17} is about half of I_{E17} (forcing Q_{20} into saturation); I_{C17}, also about half of I_{E17}, is charging C_1. Using the nominal parameters of Table 3-1:

$$I_{E17} = \frac{V \quad 0.8V}{R_{10}}$$

During this half-cycle, D_7 is reverse biased. Then V_{C13} is coupled by C_2 to the base of Q_{12}, turning it off. V_{C12} rises. D_8 goes from forward to reverse bias, D_7 goes from reverse to forward bias, and the current for maintaining D_9 in breakdown now comes from Q_{14} through D_7.

In the normal operation described above, the output voltage (V_o) has constant pulse width, and a frequency determined by V_{IN}. The significant time intervals, indicated in Figure 3-6(c), are:

$$T_1 = \frac{(C_1)(6.9v)}{(I_{C14})} = \text{constant}$$

$$T_2 = \frac{(C_2)(6.9v)}{(I_{C15})} = \text{constant}$$

$$T_3 = \frac{(C_1)(6.9v)}{(I_{C17})} = \frac{(R_{10}C_1)(6.9v)}{(V_{IN} - .9v)} = T_3(V_{IN})$$

From this, for V_o:

$$\text{Pulse width} = T_2 = \text{constant}$$

$$\text{Frequency, } f_o = \frac{1}{T_2 + T_3} = f_o(V_{IN})$$

Note that an increase in V_{IN} causes an increase in the output frequency, as required.

Now, instead of normal operation, assume that somehow the circuit of Figure 3-6(b) has become latched-up: both Q_{13} and Q_{12} are on. This means that neither V_{C12} nor V_{C13} are high enough to forward bias their respective catching diode (D_7 or D_8), and break down D_9. Hence no current is available at the base of Q_{20}: Q_{20} is cut off. With Q_{20} off, there is no path for the base current of Q_{17}, so Q_{17} must also be off. With Q_{17} off, there is no base drive for Q_{13}, so Q_{13} must be off, contrary to the original assumption (Q_{12} and Q_{13} on). In other words, latch-up is impossible, as required.

The complete circuit design, combining operational amplifier and astable multivibrator, is shown in Figure 3-7. Note that the slaved pnp current sources for the astable multivibrator (Q_{14}, Q_{15}, and Q_{16}) have their common bases connected to the common bases of the operational amplifier's slaved pnp current sources; the amplifier

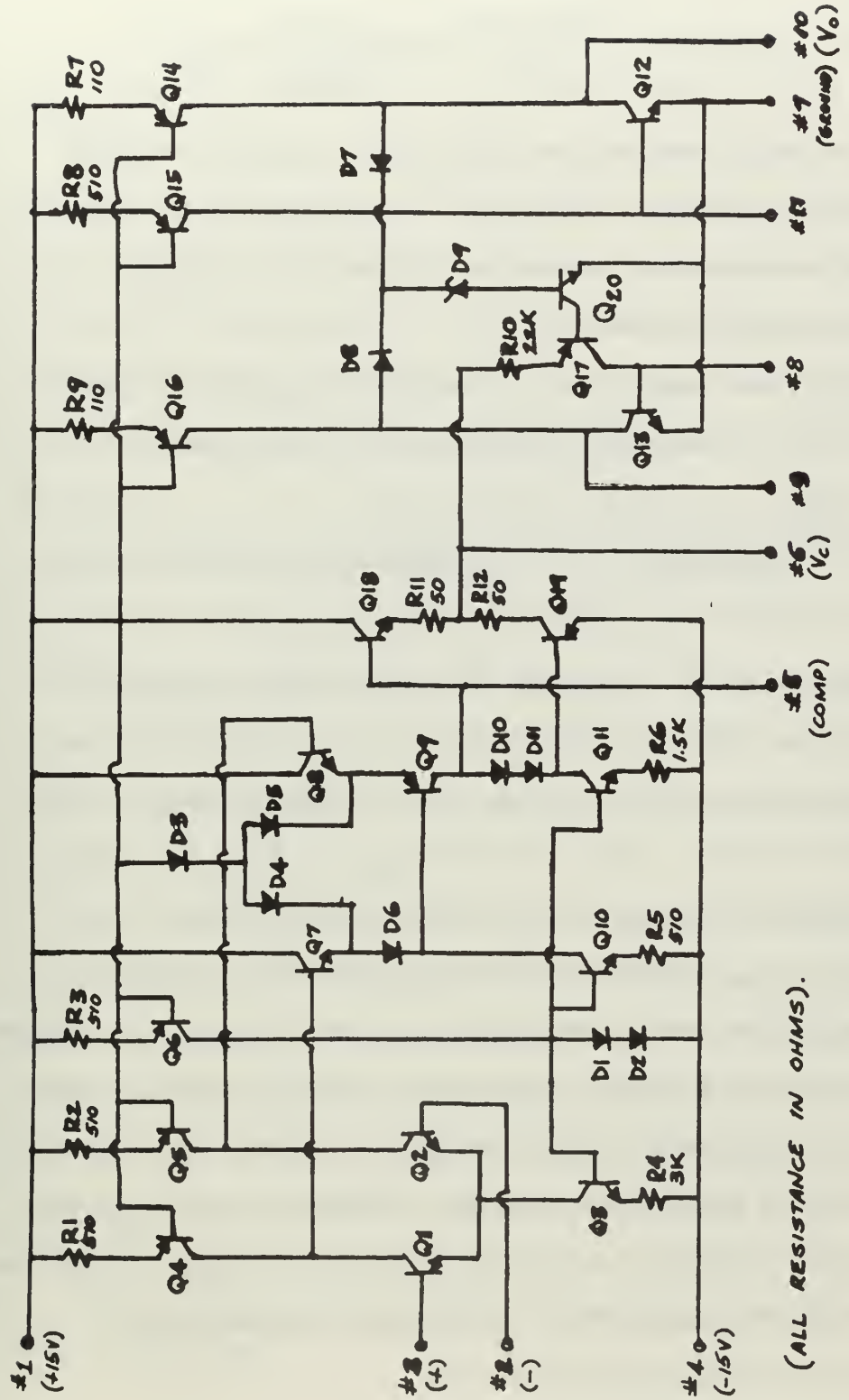


Figure 3-7: The complete circuit design for the integrated VFC.

pnp sources provide a convenient voltage point close to the positive supply voltage

Figure 3-7 shows only those components which will be part of the final monolithic chip. The astable's cross-coupling capacitors and the operational amplifier's feedback resistors and capacitor are omitted; these are external elements. The numbered nodes around the periphery of the circuit diagram indicate package pin numbers.

Three final aspects of the complete integrated VFC merit consideration: bias, external components, and frequency compensation.

It is pointed out in the preceding section that dissipation on the chip should be limited to 150 mw; at the +15V and -15V power-supply levels, this means that maximum power supply drain must be 5 ma. The resistance values listed in Figure 3-7 bias Q_1 and Q_2 each at 100 μa, Q_7 and Q_8 each at 50 μa, and Q_{14} and Q_{16} each at 500 μa. With an assumed h_{FE} of 1.0 for all lateral pnp transistors, the total power-supply drain-exclusive of Q_{17}--is 2.9 ma. Q_{17} is designed to operate at emitter currents up to .5 ma, so the total power drain is at most 3.4 ma (i.e., 102 mw dissipation on the chip). Variations in pnp h_{FE} primarily tend to redistribute, rather than increase, the current drain, so dissipation is within specifications. Changes in input voltage will require additional current momentarily to charge or discharge C_o, but such transients could reach several milliamps before dissipation became prohibitively high.

The low-current (100 μa) operating point of the input stage (Q_1 and Q_2) provides high input impedance:*

$$R_{IN} = \frac{26\, h_{FE}}{I_o\,(ma)} = \frac{(26)(50)}{(0.1)} = 13.0\,K\Omega$$

The use of the IC (Figure 3-6) with external discrete components is illustrated in Figure 3-8. Labeled voltages (e.g., "V_c") in Figure 3-8 correspond to similar quantities in Figure 2-6 and 3-7. The values of C_1 and C_2 given in Figure 3-8 were selected to provide approximately 0.5 msec pulse width and 1 KHz maximum frequency at the bias current levels listed above. For instance:

$$\text{Pulse width} = T_2 = \frac{(C_2)(6.9v)}{(I_{C15})} = \frac{(.007\,\mu f)(6.9v)}{(.1\,ma)} = .483\ msec$$

Selecting external component magnitudes for the integrator (i.e., selecting R_1, R_2, R_3, and C_o) involves two basic considerations: proper scaling for the integrator values, and minimization of offset and drift errors.

In a recent review of the use of operational integrators, Stata points out that amplifier offset and drift are the greatest sources of integrator error, and shows that (for a specified 1/RC integration factor) the smallest possible R and the largest possible C for external integrator components minimize offset and drift errors. Stata further points out that for a differential

---

*Typical input impedances for IC operational amplifiers are 10K to 500K ohms.[58]

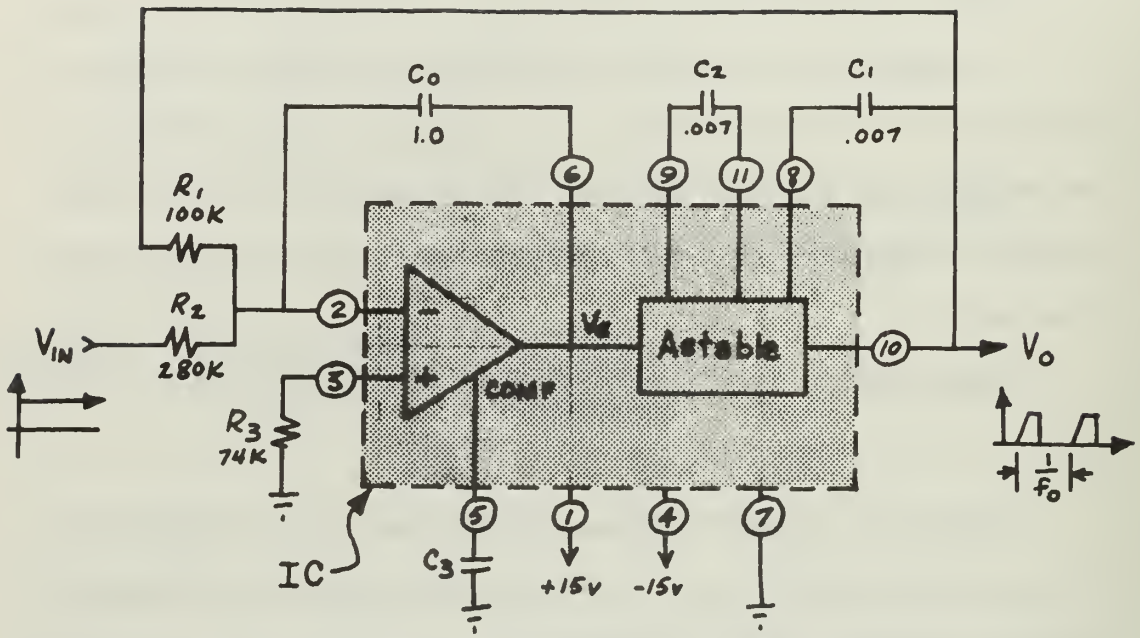


Figure 3-8: Operation of the integrated VFC.

input amplifier, offset error is in general reduced by balancing the impedance to ground as seen by each input; he notes also that 1 to 5 μf is in general a practical upper limit for capacitors.[59]

In scaling the integrator, we require that 10V input voltage corresponds to 1 KHz output frequency, and that the circuit respond rapidly to abrupt changes in input voltage. The integrator output voltage (V_c) is given by

$$V_c = \frac{1}{R_2 C_o}\int V_{IN}\,dt - \frac{1}{R_1 C_o}\int V_o\,dt$$

$$\approx \left(\frac{V_{IN}}{R_2} - \frac{\overline{V_o}}{R_1}\right)\frac{t}{C_o}$$

when the polarities of signals and amplifier gain are considered. Hence for balance at V_{IN} = 10V and fo = 1 KHz, we require approximately that

$$\frac{10v}{R_2} = \frac{3.5v}{R_1}$$

or that

$$\frac{R_1}{R_2} = .35$$

We select 1 μf as a practical value for C_o; as previously noted, 6 ma is the approximate limit for amplifier output current, due to chip dissipation constraints. Thus the maximum rate of output voltage change, neglecting amplifier limitations and loading by the astable, is

$$\left(\frac{dV_c}{dt}\right)_{MAX} = \left(\frac{1}{C_o}\right)(\text{maximum amplifier output current}) = \frac{6ma}{1\mu f}$$

$$= 6\,v/msec$$

The major restriction on the integrator resistors is the fact that R_1 is the effective load on the astable output, neglecting any other loading that use of the integrated VFC might require. For a design value, R_1 = 100 KΩ is selected to minimize loading of the astable. This requires that R_2 = 280 KΩ.

For balanced impedance at the amplifier inputs

$$R_3 = R_1 \| R_2 \approx 74\ K\Omega$$

The maximum amplifier output rate requirement occurs when V_{IN} = 10V, and V_o = 0V (e.g., when a 10V step is applied to the input); here

$$\frac{dV_c}{dt} = \frac{V_{IN}}{R_2 C_0} = .036\ V/msec$$

which is well within the maximum rate of output voltage change.

The final design problem is that of frequency compensation. The frequency response of a monolithic IC amplifier is, in general, quite complex: approximate gain expressions for direct-coupled amplifiers can be vary awkward to utilize*, and the monolithic IC parasitic effects further complicate analysis.[60] To avoid mathematical intractability, amplifier frequency response is usually measured rather than calculated, and empirical frequency compensation is then introduced; such procedure is used, for example, with the Motorola MC-1530 and Fairchild Semiconductor μA-709 operational amplifiers.[61,62] Complete discussion of monolithic operational amplifier frequency compensation is found

---

*See, for instance, the expression for output voltage, equation (21), in Motorola's application note for the MC-1530 and MC-1531 operational amplifiers.[66]

elsewhere.[63,64] Some frequency compensation is usually required to permit stable operation, and the simplest compensation scheme, providing limited amplifier bandwidth is acceptable, is to shunt some signal point to ground with a large capacitor.[65] It is this compensation method - a single shunt capacitor - which is employed in the integrator VFC's operational amplifier, as shown in Figures 3-4 and 3-7; the resultant decrease in amplifier bandwidth is completely acceptable, since the integrator is a low-pass filter which we are only using to integrate the DC component of V_o. No value is indicated in Figure 3-8 for the compensation capacitor (C_3); this value is determined empirically, as explained above.

Temperature compensation is discussed in the next section; it is primarily a mask design problem, rather than a circuit design problem, for the integrated VFC.

4. CIRCUIT EVALUATION

As pointed out in the Introduction, the final task of the IC designer is to evaluate his circuit design; such evaluation may indicate circuit modifications, after which the modified circuit is again evaluated. IC evaluation terminates only when the design is satisfactory.

Evaluation of an IC design must be accomplished in two areas: First, the electrical performance of the IC design must satisfy the original specifications. Second, the design must be economically feasible; i.e., area requirements for the IC must be sufficiently low to make it competitive in price.

In this section we evaluate the integrated VFC design. Measurements are made with an equivalent discrete circuit breadboard to indicate performance of the eventual VFC IC. The thermal sensitivity of the integrated VFC is discussed. Finally, economic feasibility is investigated by tabulating area requirements for the IC, and by constructing a rough circuit layout. Normally the IC designer is not concerned with mask layout,[1] but the rough layout is included here to indicate the form of the final IC.

BREADBOARD PERFORMANCE

At some point in the design of any electronic circuit, a breadboard model is constructed to provide, hopefully, realization of the theoretical design parameters. With monolithic IC's, breadboard evaluation acquires even greater significance than with discrete circuits, because detailed theoretical analysis of a monolithic IC is generally not feasible;[2] moreover, an IC breadboard permits measurements which might be difficult or even

impossible to perform on the chip, and permits circuit modifications which are typically lengthy and very expensive to accomplish on the production line. Several IC manufacturers - notably Fairchild,[3,4] Motorola,[5,6] and Signetics[7] - appear to favor the discrete component breadboard, while Westinghouse advocates selective wiring of a multi-component master chip.[8]

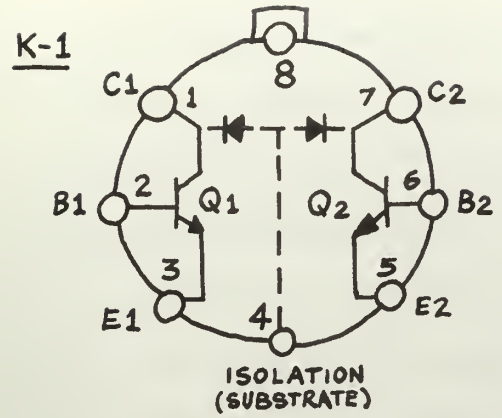
Regardless of the approach used, the objective of breadboarding remains the same: close approximation, prior to mask design and IC production, of the eventual IC. The easiest breadboard to construct is one using only discrete components; however, a completely discrete breadboard avoids most of the parasitics which will be encountered on the chip (and possibly introduces parasitics which will not be found on the chip), and does not provide testing of bias for the critical component-to-substrate isolation diodes. At the other extreme, the most difficult breadboard to construct is one using a form of master chip; nonetheless, the master chip breadboard probably provides the closest electrical simulation of actual IC performance.

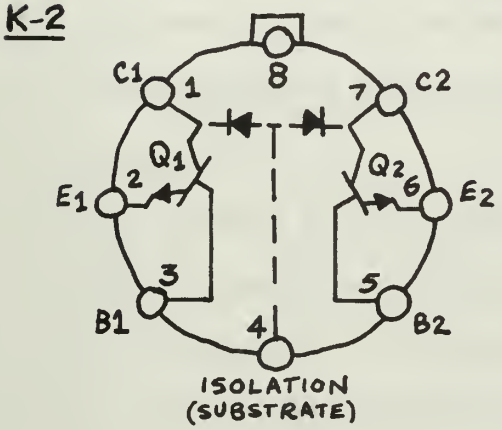
The breadboarding method used in this investigation is a compromise between the two extremes above: we use monolithic IC components for all active devices, together with standard discrete resistors. This method provides a better evaluation of parasitics and isolation than is possible with a totally discrete breadboard, while avoiding the difficulties in circuit modification and testing presented by the master slice breadboarding approach.

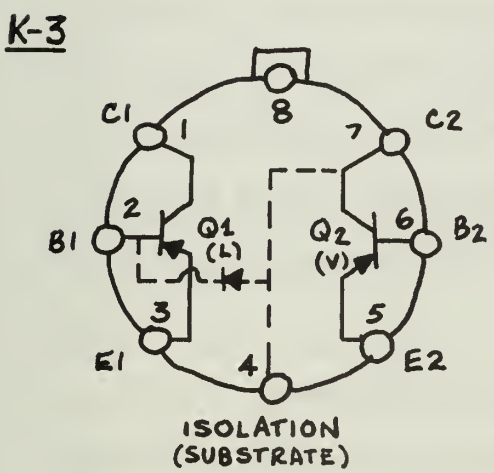
Fairchild Semiconductor provided "kit parts" for use in the integrated VFC breadboard; these consist of monolithic IC transistor

pairs mounted in modified (8-lead) TO-5 cans. Figure 4-1(a) shows the connection diagrams for the three kit parts - designated K-1, K-2, and K-3 in this thesis - used in the integrated VFC breadboard. K-1 and K-2 are virtually identical, except for the lead numbering: each consists of a matched pair of adjacent npn transistors. K-3 consists of a lateral and a vertical pnp transistor; since the vertical pnp collector is the substrate,these are shown common in Figure 4-1(a). Typical measured output characteristics for K-1, K-2, and K-3 are provided in Figure 4-1(b). Note the characteristically lower h_{FE} for the lateral pnp than for the vertical pnp transistor.

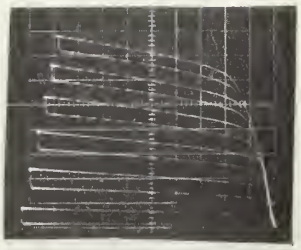
The major difference between the kit part breadboard and the monolithic IC which it models, is size: the breadboard is necessarily many times larger than the IC. Components in the actual IC are very close (at worst, on the order of 50 mils apart), and share a physically common substrate. This close spacing means that temperature gradients between components are virtually negligible. All portions of the IC are at essentially the same temperature, while significant temperature differences can exist between breadboard components. Accordingly, breadboard measurements of the temperature dependence of circuit performance are of questionable relevance in evaluating the IC design.[9] However, a monolithic IC is much more sensitive to temperature than a typical discrete circuit, so rough measurements of breadboard temperature sensitivity can be helpful, provided that their limitations are considered.[10]

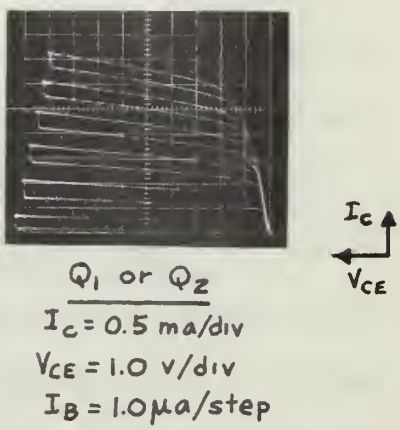


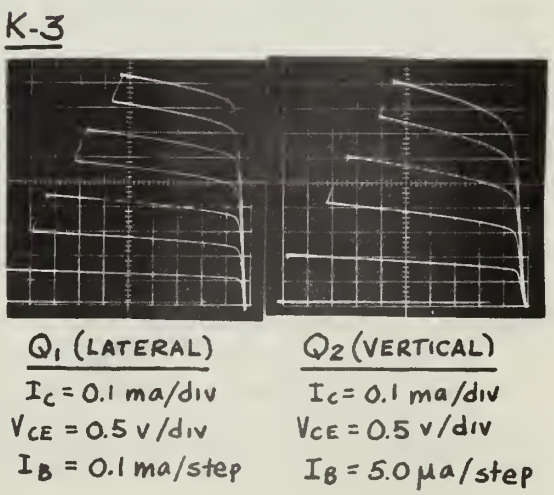




(a). Connection diagrams (top view).







(b). Output characteristics.

Figure 4-1: Fairchild Semiconductor kit parts used in the integrated VFC breadboard.

Size differences between the IC and its breadboard introduce another modeling inaccuracy, due to conductors. Compared to the IC metallization, breadboard conductors are very long and thick, and so the breadboard may have parasitic effects (notably parasitic inductance) which are never found on the chip. It is essential that the breadboard be as small as possible, with short leads.

Another possible breadboard/IC dissimilarily is component matching. Both kit parts and discrete resistors must be carefully chosen so that their values are within monolithic parameter magnitude and ratio tolerances.

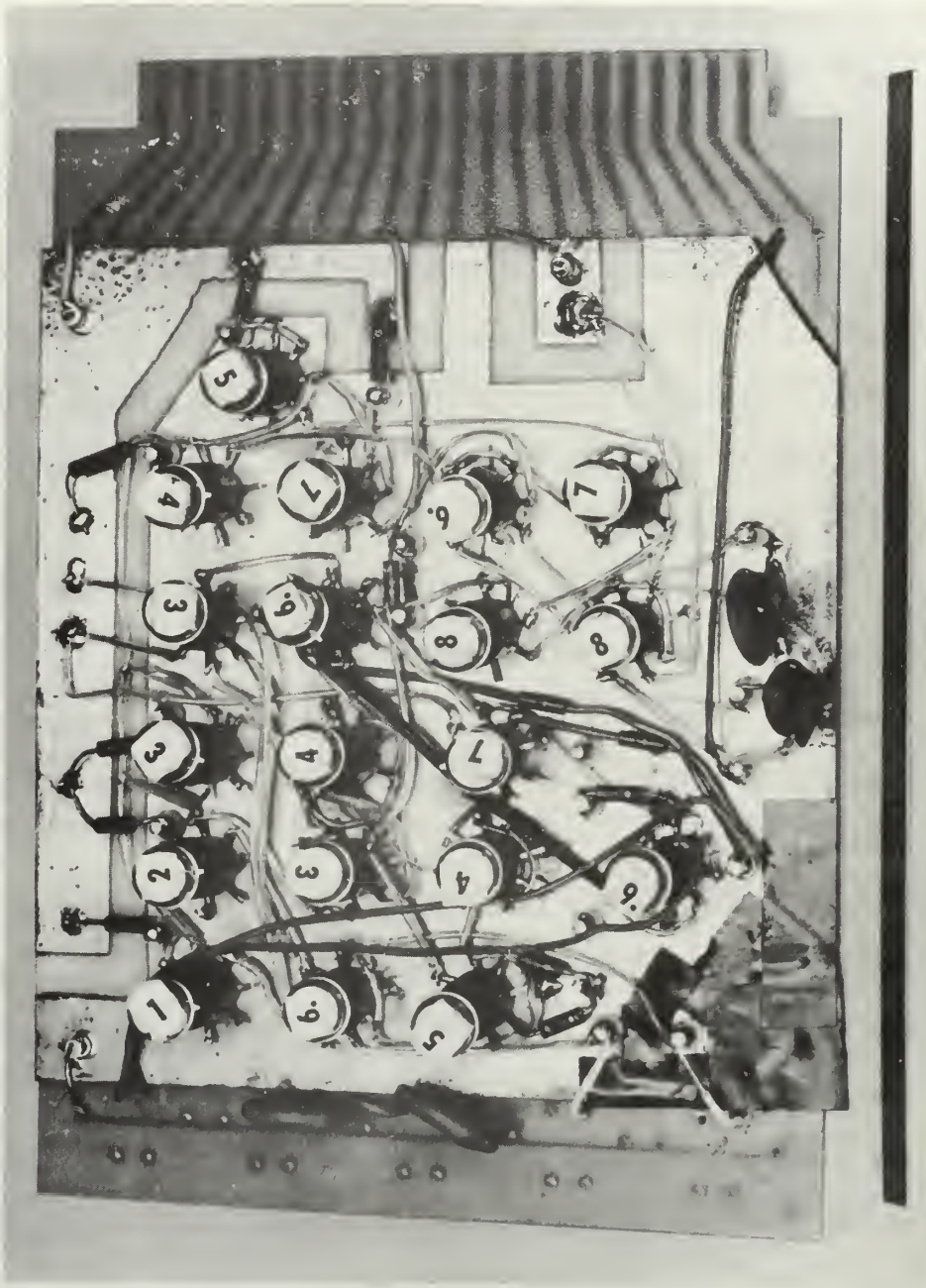
The integrated VFC breadboard is constructed as shown in Figure 4-2. The breadboard was initially built on etched copper-clad printed circuit board; the copper-clad board is presently mounted on a plug-in card to facilitate interconnections. Its small size makes the breadboard relatively unaffected by connector parasitics. The kit parts of Figure 4-1 are used for all active devices; diodes, including the Zener diode (D_9), are formed by suitable external connection of transistor leads. Wiring details are omitted from Figure 4-2 for clarity; the breadboard is wired exactly as shown in Figure 3-7.

All cans shown in Figure 4-2(b) are K-1 (npn pairs) or K-3 (pnp pairs) kit parts, as appropriate, except for those cans marked with an asterisk (e.g., $Q_{7/8}$ in Figure 4-2(b)) which are K-2 kit parts; the numbers on top of the cans in the breadboard photograph, Figure 4-2(a), indicate different units in each of the K-1, K-2, and K-3 kit part types.

Figure 4-3 shows the final circuit configuration used for the VFC. The package connection diagram, Figure 4-3(a), is based on the rough circuit layout described in the next section, and the modified (12-lead) TO-5 package required by the specifications. The external components used to complete the integrated VFC are shown in Figure 4-3(b). The values of the external components were all optimized experimentally; note the agreement of the experimental values of Figure 4-2(b) with the estimated values listed in Figure 3-8.

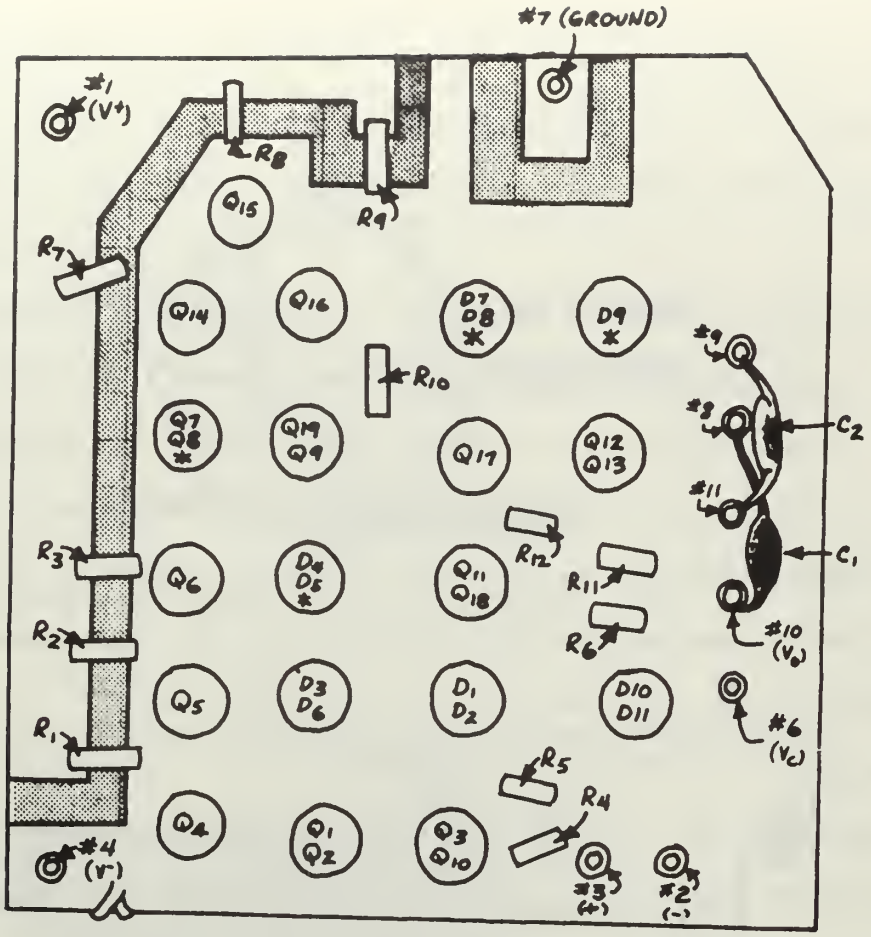
Several components are shown in Figure 4-2(b) that are not included in Figure 3-8: capacitors C_4, C_5, and C_6; and clamping diode D_1. Capacitors C_4 and C_5 are power supply by-pass (decoupling) capacitors, which are essential with any high-gain feedback amplifier.[11]

If a sufficiently high positive signal is applied to the inverting input of the amplifier, Q_2 will saturate (see Figure 3-7) and appear as a small incremental resistance to the signal; with the signal inversion of Q_2 no longer in the signal path, the inverting input then becomes a mon-inverting input, and the high gain of the amplifier causes the output to saturate (i.e., V_c goes to about +15V), possibly with destructive current levels. The integrator is particularly susceptible to this type of latch-up, since an output transient is directly coupled to the inverting input by the feedback capacitor C_o. Using the input clamping diode D_1 obviates this latch-up possibility.[12]



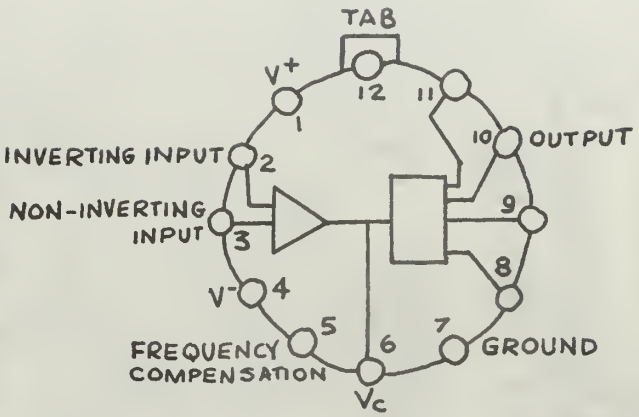
(a). Photograph.

Figure 4-2: The integrated VFC breadboard.

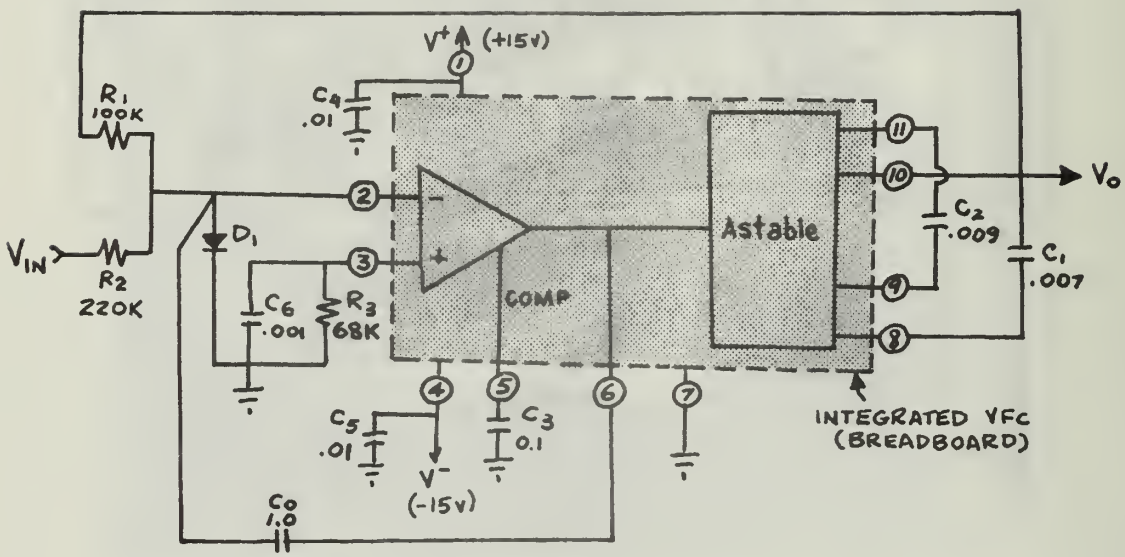


(b). Component identification.

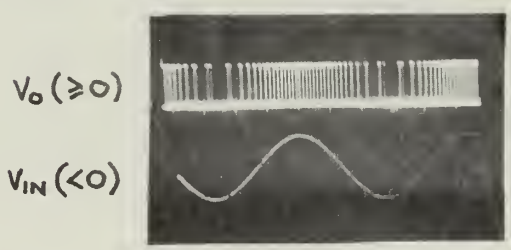
Figure 4-2: The integrated VFC breadboard.



(a). Package connection diagram (top view).



(b). Circuit diagram.



(c). V_O, V_{IN} waveforms.

Figure 4-3: Final configuration and waveforms for the integrated VFC.

Finally, the non-inverting input bypass capacitor C_6 compensates for the parasitic input capacitance at this terminal; without C_6 the parasitic capacitance would possibly cause high frequency oscillations.[13]

Breadboard performance is summarized in Figure 4-4 and Table 4-1. Two sets of kit parts were used to determine breadboard susceptibility to random variations in component parameters.

As shown in Table 4-1, amplifier open loop gain, offset, and offset drift were among the performance parameters measured. These measurements are fairly straightforward and amply described elsewhere.[14,15] The results of these measurements roughly describe the performance of the integrated VFC's amplifier portion; however, since the amplifier is necessarily disconnected from the astable during these measurements, the actual performance of the amplifier on the closed-loop VFC may be somewhat different from that indicated in Table 4-1.

Table 4-1 also lists overall performance data for the VFC circuit shown in Figure 4-3; the circuit transfer characteristic is provided in Figure 4-4.

There is a significant artificiality which must be considered when evaluating both the amplifier performance data and the overall VFC performance data: the discrete resistors in the VFC IC breadboard were limited to standard values so that the precise bias levels of the design could not be set. The data in Figure 4-4 and Table 4-1, especially when the resistor artificiality is noted, show that the circuit design of Figure 3-7, used in the circuit of Figure 4-3(b), is an electrically feasible solution to the design specifications listed in the previous section.

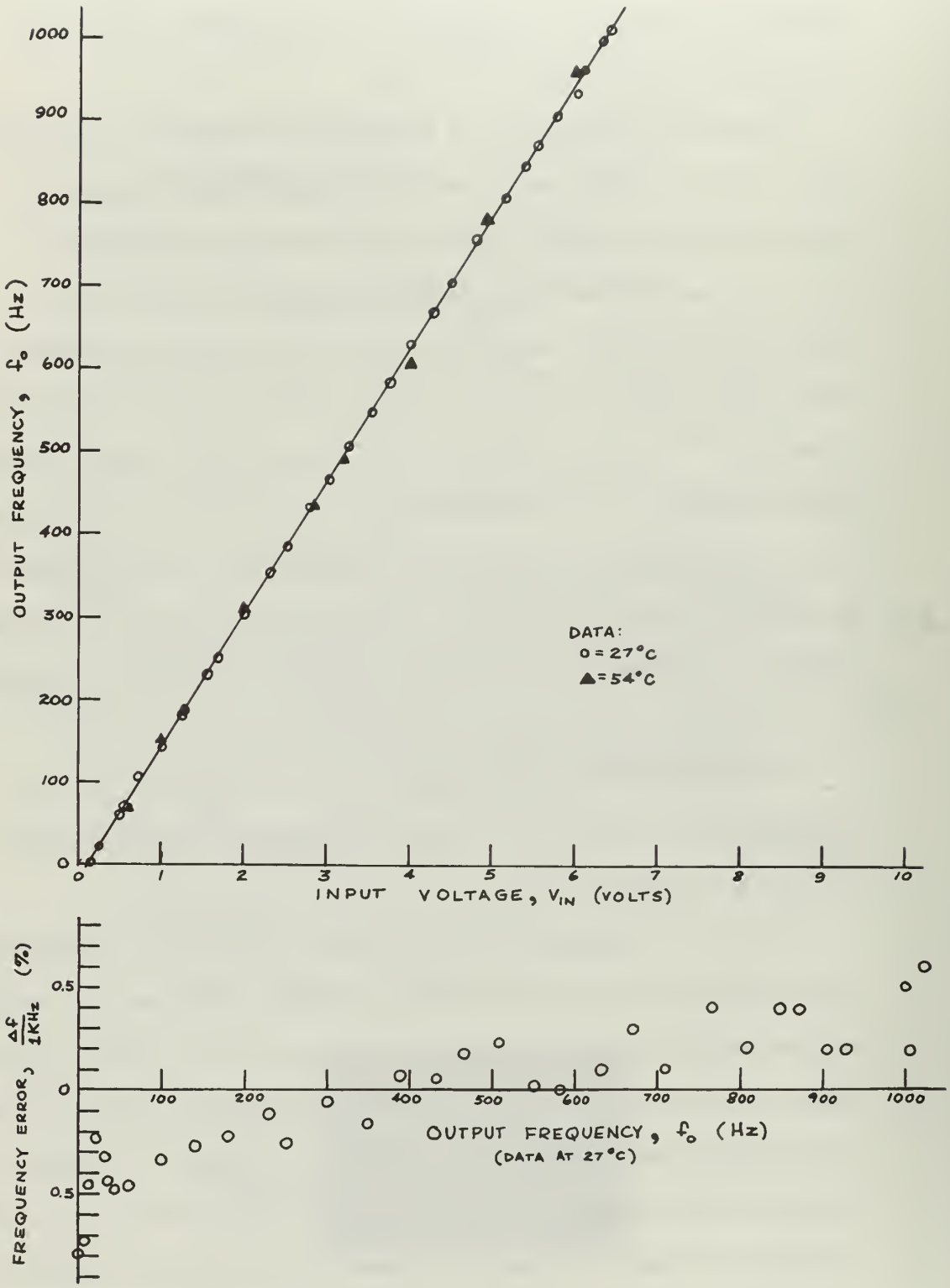


Figure 4-4: Breadboard transfer characteristics for the integrated VFC.

Table 4-1

BREADBOARD PERFORMANCE SUMMARY FOR THE INTEGRATED VFC

(a) Amplifier data

	Parameter	Value	Notes[a]
(1)	Open-loop gain	75 db	
(2)	Input offset voltage	8.05 mv	
(3)	Input offset voltage drift	35.9 μv/^{o}C	(b)

(b) VFC Data

	Parameter	Value	Notes[a]
(1)	Output frequency range	0-1 KHz	(c)
(2)	Maximum output frequency change	2000:1	
(3)	Voltage-to-frequency conversion factor	160 Hz/v	
(4)	Linearity	0.8%	(d)
(5)	VFC input offset voltage	151 mv	(e)
(6)	Output frequency sensitivity to supply voltage variations	+0.6%/v	(f)
(7)	Output frequency drift	0.18%/^{o}C	(b), (g)

(a) All measurements at T = 27^{o}C except as noted.

(b) Measured to T = 54^{o}C.

(c) Actual minimum non-zero frequency was 0.5 Hz.

(d) Minimum (per cent of full-scale) from 0 to 1 KHz.

(e) Maximum input voltage for zero output frequency.

(f) Average from $\pm$ 12v to $\pm$ 17v.

(g) Maximum magnitude (per cent of full scale) from 0 to 1 KHz.

THERMAL CONSIDERATIONS

In order for the integrated VFC to be relatively insensitive to temperature variations, the circuit must provide essentially error-free integration of a pulse train whose average value is virtually independent of temperature.

Integration is essentially error-free if the integrator offset voltage and current are negligible: the combined voltage and current offset constitute a ramp error at the integrating output. External minimization of integrator offset involves selecting a large feedback capacitor C_o and small input resistors R_1 and R_2, and balancing impedances seen at the inverting and non-inverting inputs as discussed above. Offset minimization within the amplifier involves matching the input transistor pair Q_1 and Q_2, the input stage current sources Q_4 and Q_5 (with their resistors R_1 and R_2), and the second stage emitter followers Q_7 and Q_8; this matching is done by proper mask design. Offset drift, assuming component matching with temperature tracking, is primarily a CM effect; the large CM rejection of the VFC amplifier largely eliminates drift error.

Maintaining a constant average value for the V_o pulse train as temperature varies is a more complicated problem than error-free integration. The controlled current source--Q_{17} and its related components--represents no problem: assuming error-free integration and otherwise temperature-independent operation, any error in V_o due to temperature variation effects on the controlled current source would only be an error in frequency, since the

controlled current source affects only the inter-pulse interval; thus error due to temperature variation effects on the controlled current source would be eliminated by the proportional-error loop. For instance, assume that temperature changes made I_{C17} too high, which would cause the output frequency f_o to be too high. Then the average value of V_o, $\overline{V_o}$, would similarly be too high, and the integrator would ramp down to the value of V_c which produced the correct f_o. There are two primary factors which can produce frequency error due to temperature variation: the operation of constant current sources Q_{14} and Q_{15}, which vary similarly with temperature; and the value of V_{C12} when Q_{12} is off. The CM rejection in the amplifier tends to eliminate temperature-caused changes in signal point potentials, so the collectors of Q_1 and Q_2 stay at an approximately constant voltage as temperature varies. Since the base bus line for the slaved pnp current sources is essentially above $V_{C1}(=V_{C2})$ by the voltage across D_3, the base-to-ground voltage V_{B14} and V_{B15} have the same positive temperature coefficient as the voltage across D_3. The base-to-emitter voltages V_{BE14} and V_{BE15} also have a positive temperature coefficient, so the emitter voltages V_{E14} and V_{E15} have a resultant positive temperature coefficient; for instance, as temperature increases, V_{E14} and V_{E15} become more positive--i.e., move closer to the positive supply voltage--which tends to decrease I_{E14} and I_{E15}, and thus decrease I_{C14} and I_{C15}. The resistors associated with Q_{14} and Q_{15}, R_7 and R_8,have positive temperature coefficients and so resistor thermal variations have the same sort of effect as V_{E14} and V_{E15} on astable operation; for instance, an increase in

temperature tends to increase R_7 and R_8, and thus tends to lower I_{C14} and I_{C15}. The increase in h_{FE} with temperature offsets these current decreases somewhat, but typically thermal variations of I_{C14} and I_{C15} are inverse in nature: an increase in temperature tends to decrease both I_{C14} and I_{C15}, and vice versa. Any decrease in I_{C14} decreases the output average value $\overline{V_o}$, since I_{C14} directly determines the duration of the ramp on the leading edge of V_o (see Figure 4-3(c)). Conversely, a decrease in I_{C15} causes an increase in pulse width, and hence an increase in $\overline{V_o}$

The pulse height depends on the voltage across D_7, D_9, and Q_{20} when Q_{12} is off; since both the voltage across D_7 and $V_{CE20(sat)}$ have positive temperature coefficients, while the voltage across the Zener diode D_9 has a negative temperature coefficient, the resultant pulse height--and hence $\overline{V_o}$--can be made to have a positive, negative, or nearly zero temperature coefficient.

It can be seen from the preceding remarks that temperature variation produces a variety of opposing changes in parameter variations; with appropriate selections of component geometries, these opposing changes can be made to almost cancel, so that the VFC output frequency is virtually insensitive to temperature.

CIRCUIT LAYOUT

As mentioned above, area requirements for an IC design constitute an essential criterion of the IC's economic feasibility. Appendix II lists 60 mils square as the typical maximum area for reasonable yield with a monolithic IC. Hence a necessary part of

IC design evaluation is tabulating the area requirements for the IC. As stated in the Introduction, this tabulation is generally the final role of the electronics engineer in IC design.

We first list the geometrical constraints on monolithic IC components, next formulate monolithic layout rules, and then examine a rough circuit layout for the integrated VFC. Although a purely numerical determination of area requirements for the integrated VFC would have been sufficient for this phase of design evaluation, we use the rough layout because it facilitates visualization of the completed product. The information on component geometry and layout rules was compiled from several sources, which are in surprising agreement, considering the proprietary nature of the details of such information.[16-22]

Monolithic IC component geometry is primarily determined by tolerances, since area minimization is the prime objective of IC layout. Geometry constraints can be loosely grouped into three categories: clearances (spacing between IC elements and components), stripe widths (widths across long, narrow IC elements), and areas (for IC components). These constraints are summarized in Table 4-2.

Monolithic IC layout is essentially two-dimensional; as pointed out in the layout rules listed below, three-dimensional structures (e.g., crossovers) are generally undesirable since they degrade circuit performance. Thus monolithic geometry constraints are cast in terms of the IC surface arrangement: clearances, stripe widths, and areas. We use "stripe" to refer to both long, narrow physical regions - such as "emitter stripes" and "metallization

Table 4-2

TYPICAL MONOLITHIC GEOMETRY LIMITS

(a) Clearances

	Location	Minimum (mils)
(1)	Metal to base-emitter junction	0.25
(2)	Metal to metal	1.00
(3)	Chip edge to junction	3.00
(4)	Chip edge to bonding pad	1.00
(5)	Isolation region to isolation stripe	1.00
(6)	Contact hole to junction	0.25
(7)	All others	0.50

(b) Stripe widths

	Type	Minimum (mils)
(1)	Transistor emitter	1.00
(2)	Diode emitter	0.75
(3)	All others	0.50

(c) Areas

	Device	Minimum (mils by mils)
(1)	Transistor[(a)]	4.0 by 5.0
(2)	Diode[(a)]	3.5 by 4.5
(3)	Bonding pad	3.0 by 3.0

(a) To edge of isolation region.

(connector) stripes" - and long, narrow areas on the masks - such as "isolation stripes"; sometimes the terms "line" and "line width" are used in the literature in place of "stripe" and "stripe width" respectively.[23]

The minima listed in Table 4-2 are typical for monolithic IC's with moderate yield. There is a trade-off between tolerance and geometry minima: the minima of Table 4-2 provide a certain yield for a specific set of circuit tolerances, and the same yield could be maintained with smaller minima if the tolerances were relaxed somewhat.

The size of transistors is set by current ratings. The 4 x 5 mil transistor area listed in Table 4-2 is the minimum area possible, and is suitable for collector currents up to about 6 ma; for currents in excess of 6 ma, 3 mil^2 is required for each milliamp of collector current.

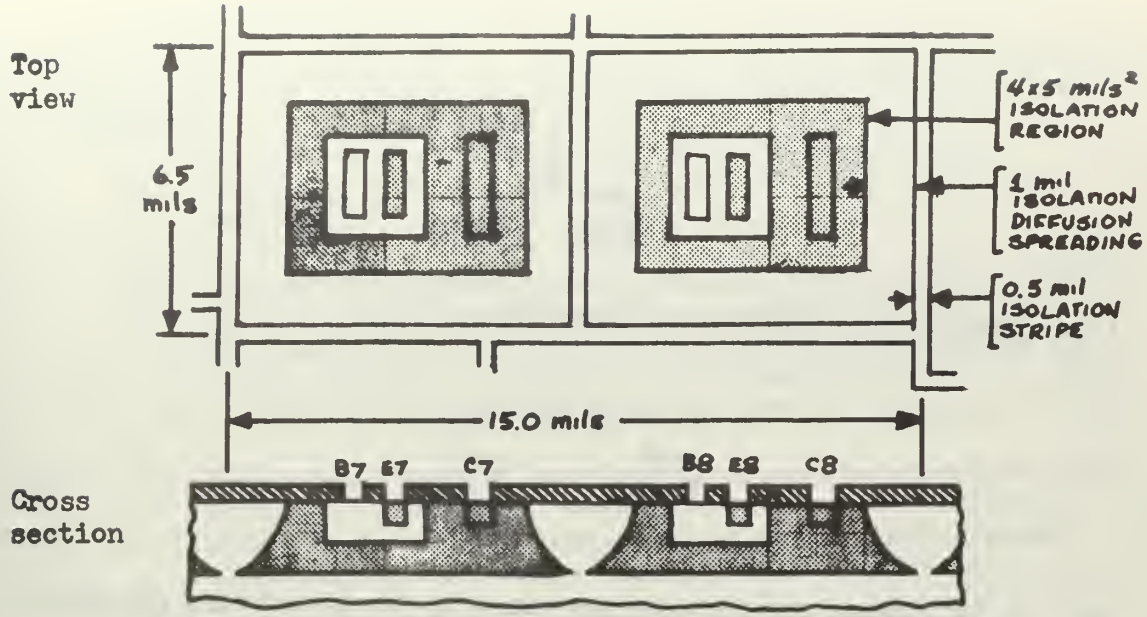
Table 4-2 emphasizes the importance of minimizing the number of isolation regions in a given circuit. Since the isolation diffusion must cross a one mil wide epitaxial layer, and since diffusions move about the same distance in all directions (see Appendix II), the isolation diffusion extends approximately one mil to either side of the isolation stripe. Thus adjacent components in separate isolation regions have a wide separation (2.5 mils) which is eliminated when these components are combined into a common isolation region.

Base diffusion resistors can be combined in a single isolation region without affecting their isolation; combining npn and vertical pnp transistors (and diodes) is possible only when their collector

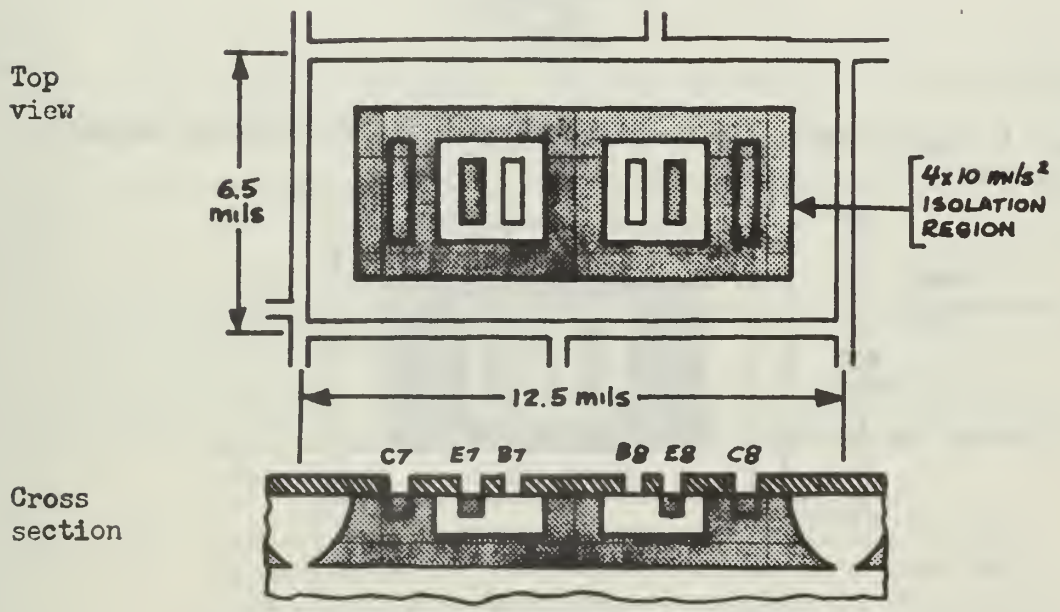
regions are at a common potential, while lateral pnp transistors can be combined only if their bases are common. For instance, the Q_7/Q_8 common collector pair in the integrated VFC circuit (Figure 3-7) can occupy a common isolation region. Figure 4-5 illustrates the area reduction achieved when Q_7 and Q_8 are combined into a single isolation region: with Q_7 and Q_8 minimum geometry transistors (4 by 5 mils) as shown in Figure 4-5, the common isolation region configuration occupies an area of 81.25 $mils^2$, compared to the 97.50 $mils^2$ required for separate isolation regions; this is an area reduction of almost 17 per cent. Note that the area reduction is shown for the original transistor geometries merely moved together; further geometry modification, such as eliminating a collector stripe, would provide additional area reduction. Overall dimensions and areas are measured to the center of isolation stripes.

Further geometry variations are possible. For example, consider diodes D_4 and D_5 in the integrated VFC design, which are connected as shown in Figure 4-6(a). These diodes could be realized with a pair of transistors connected as high speed diodes (Figure 4-6(b)). However, minimum area is used when D_4 and D_5 are formed by a double-emitter transistor (Figure 4-6(c)); the area requirement for the single transistor realization is shown in Figure 4-6(d).

Bonding pad area is determined by the size of the wire used to connect bonding pads to the package pins and by the method of bonding used. The 3 by 3 mils pad area listed in Table 4-2 is the minimum where 1 mil wire is used; to facilitate the manual bonding process, larger pads--such as 6 by 6 mils--are more common.[24]



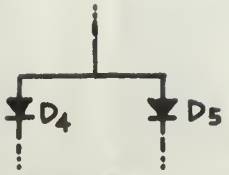
(a). Q_7 and Q_8 in separate isolation regions.



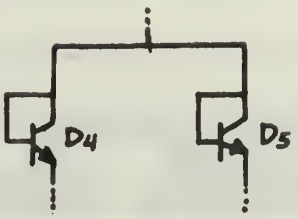
(b). Q_7 and Q_8 in a common isolation region.

Figure 4-5: An example of chip area reduction through the use of a common isolation region.

(Not to scale; buried layer and metallization omitted).

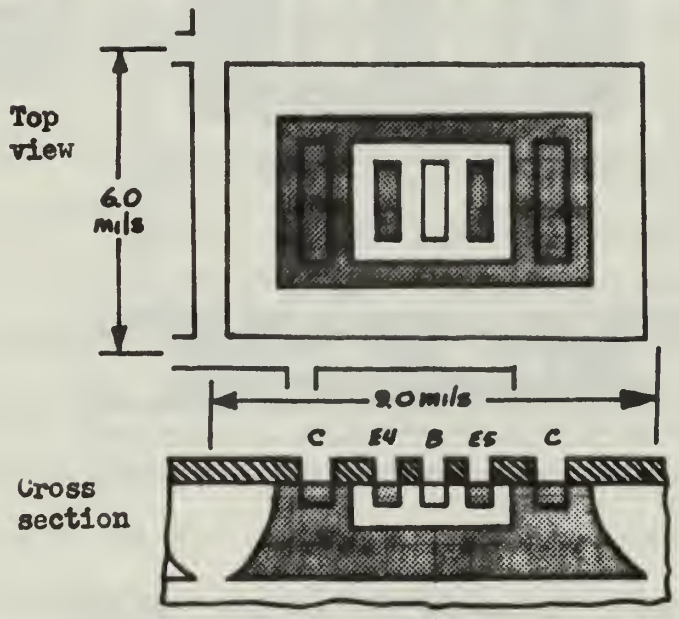


(a). The circuit requirement (from Figure 3-7).



(b). A two transistor realization (used in the breadboard circuit).

(c). A single transistor realization (used in the circuit layout).



(d). Layout for the single transistor realization.
(Not to scale; buried layer and metallization omitted).

Figure 4-6: Development of a minimum geometry device.

Monolithic IC layout rules follow directly from the various constraints of the monolithic technology. The following sequence is typical:

(1) Determine any pin connections specifically required of the IC.

(2) Develop the rough IC layout by drawing a circuit schematic with leads in the same order as required by specified pin connections, if any; if at all possible, decide on pin connections only after the schematic has been revised to account for crossovers and isolation regions.

(3) Determine crossover requirements from the schematic, and eliminate crossovers wherever possible; use resistor crossovers in preference to metal-oxide-semiconductor (MOS) crossovers, since the latter have worse parasitics.

(4) Determine isolation regions and minimize the number of isolation regions by grouping components in common isolation regions where feasible; however, do not use very large isolation regions, to avoid leakage and parasitic capacitance problems.

(5) Assign any remaining pin connections.

(6) Design IC component geometry to satisfy circuit performance requirements in minimum area.

(7) Arrange components to provide uniform power dissipation over the chip surface.

(8) Where component matching is required, use identical geometries and proximate locations at chip isotherms for the matched components.

(9) Subject to component spacing constraints, minimize the area of the entire IC layout, to achieve low parasitic capacitance and high yield.

(10) Connect the substrate to the most negative voltage appearing on the chip, and connect the n-type (epi) region around base-diffusion resistors to the positive supply voltage, to reduce distributed capacitance and leakage.

(11) Position bonding pads at the IC periphery, so that the bonding tool does not have to pass over the chip; do not place pads over buried components, nor such that wires from the pads to the package pins would cross.

(12) Minimize the length and number of metallization connector runs across isolation regions.

The VFC IC layout, Figure 4-7, compiles with the preceding layout rules and geometry constraints. As discussed above, the purposes of this layout are to show the economic feasibility of the IC design and to indicate the approximate configuration of the eventual IC. For clarity, details such as interconnection locations and diffusion edges have been omitted; instead, Figure 4-7 shows isolation region edges as what would actually be center lines for the isolation stripes. Transistor and diode orientations are indicated roughly; for example, compare device details for Q_7 and Q_8 (Figure 4-4) and for D_4 and D_5 (Figure 4-6) with the device locations in Figure 4-7. Details are shown for R_{10}, R_{11}, and R_{12}, since these represent extremes in geometry: R_{10} is by far the largest resistor in the circuit, while R_{11} and R_{12} are so small that they must be wider than the .5 mil width used for other resistors in the IC.

The rough layout in Figure 4-7 comprises a 48 by 52 mil chip, divided as follows:

Transistors and diodes	1,264 mil^2
Resistors	196 mil^2
Pads (excluding overlap)	663 mil^2
Waste Area	373 mil^2
Total area	2,496 mil^2

Thus, in spite of the required "waste" area outside the pads, there is less than 15 per cent waste; moreover, active devices (transistors and diodes) use more than five times as much area as resistors.

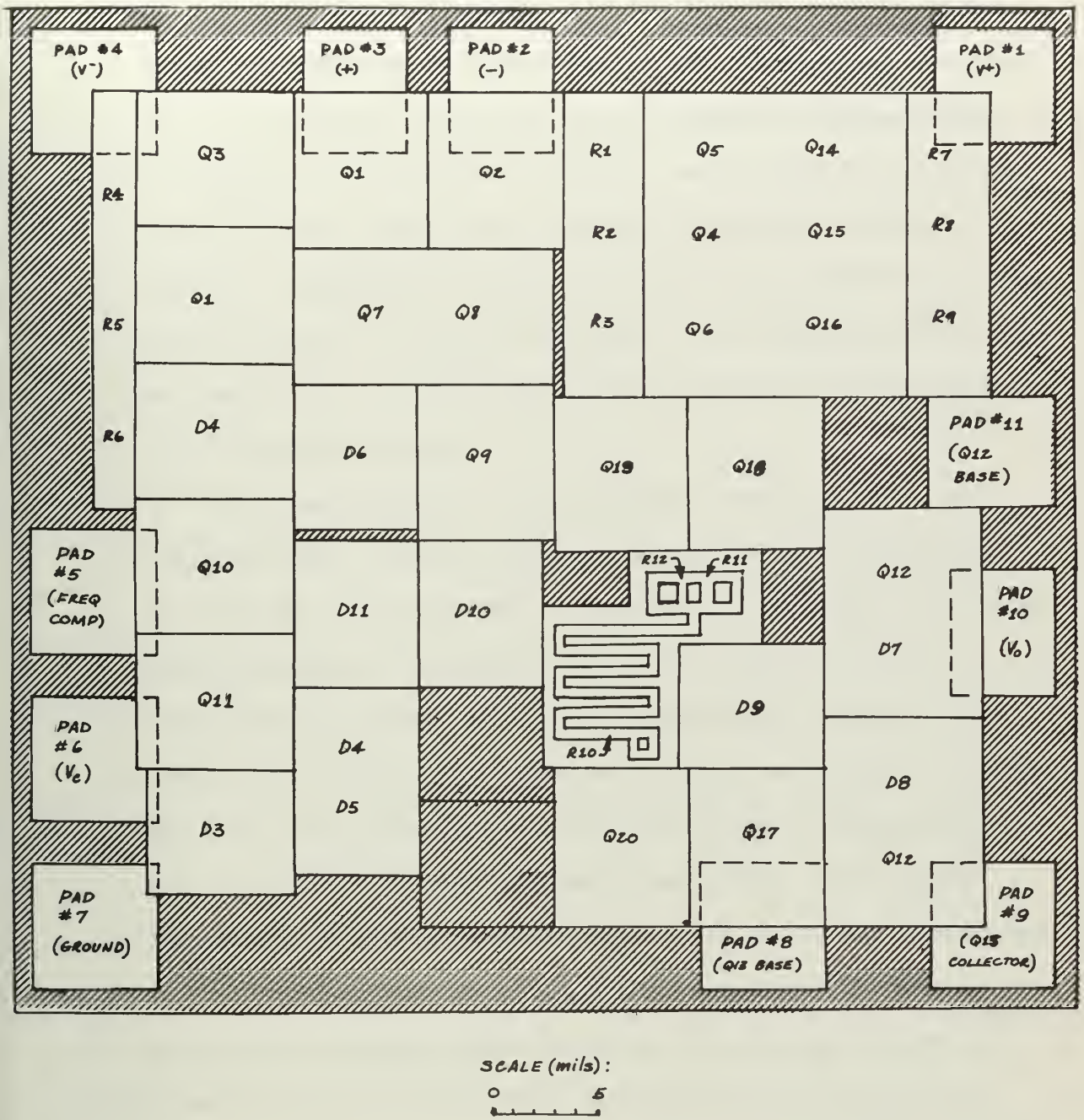


Figure 4-7: Rough circuit layout for the integrated VFC.

Since about 65 by 65 mils is the current upper limit for chip size, we may conclude that the 48 by 52 mil integrated VFC layout is economically feasible.

5. SUMMARY AND CONCLUSIONS

In preceding sections the various phases of monolithic IC design are examined in some detail, on two planes simultaneously: first, the general aspects of the monolithic IC design process are considered and, wherever possible, these general aspects are formalized into design rules and typical parameters; second, the design of a specific monolithic IC--the integrated VFC--is evolved, using the general design methodology. It is appropriate then that we consider the results of this thesis separately for the general and the specific problem.

The general problem - describing the total monolithic IC design process - has been covered extensively in the literature, as evidenced by the quantity of references accompanying this paper. However, monolithic IC design literature tends to be limited in each instance to a portion of the design process: fabrication details are found in some references, design techniques in others, and still other references indicate trends while presupposing reader knowledge of both fabrication and design. And in many instances, monolithic IC literature is cast in its own terminology. In this paper we have instead a unified treatment of the complete monolithic IC design process, together with definitions for the prevalent IC terminology, and a description of trends in, and fabrication of, the monolithic IC. Based on our unified treatment, we can draw three essential conclusions:

First, knowledge of monolithic IC fabrication is essential in understanding and working within monolithic IC design constraints.

Second, once fabrication and design constraints are understood, monolithic IC design becomes a fairly simple process: under the stringent component limitations and equally stringent design constraints, ingenuity is virtually the only degree of freedom available to the monolithic IC designer.

Third, monolithic IC design in an organization which is not a monolithic IC manufacturer requires a close working relationship between the organization and an IC manufacturer, since IC fabrication presently involves standard production lines which differ in different IC manufacturers, and since the IC designer requires information on many production details, such as device performance and tolerances, which are often proprietary.

The specific problem--design of an integrated VFC for industrial control applications--serves to illustrate monolithic IC design; moreover, the final VFC design is a practical possibility for monolithic production. A survey of VFC methodology and theory (Section 2) indicates that the functional arrangement chosen for the VFC (Figure 2-6) is a near-optimum selection. The circuit design (Figure 3-7) is in accordance with the various design constraints (Section 3). And, most important, evaluation of its electrical performance and economic feasibility showed that the integrated VFC performed satisfactorily and could be readily realized in integrated form. Four aspects of the integrated VFC design merit amplification:

First, the electrical performance of the circuit breadboard, summarized in Table 4-1 and Figure 4-4, might appear marginal in terms of the VFC design specifications. However, with suitable optimization--especially with proper mask design, as discussed in relation to thermal considerations (Section 4)--performance should meet the specifications.*

Second, the chip size (48 by 52 mils) is entirely satisfactory; for comparison, the Fairchild A709 monolithic operational amplifier is built on a 55 by 55 mil chip,[1] and sells for $6.60 (0 to 55°C rated temperature range, TO-5 package, 100-999 quantities).[2]

Third, a significant market exists: the integrated VFC would provide equivalent performance with reduced size and price and increased reliability, when compared to present VFC's in the area of industrial control; additionally, the integrated VFC compares favorably with discrete laboratory VFC's, and probably would satisfy requirements in many of the numerous other VFC applications (Section 2). In other words, an IC--the integrated VFC--which is designed for a single purpose in a single market, constitutes an excellent possibility for high-volume monolithic production.

Fourth, the integrated VFC design points out the necessity of design ingenuity in developing monolithic IC's: a unique circuit design--for voltage-control of the astable multivibrator--is essential in achieving the desired integrated VFC performance.

---

*Performance data is based on the circuit of Figure 3-7, except that the base and collector leads of Q_{20} were interchanged; this modification provides equivalent performance, but may be subject to latch-up.

REFERENCES

SECTION 1. INTRODUCTION

1. Murray Siegel, Manager of Test Measurements and Control Applications, Fairchild Semiconductor. (Personal interview).

2. D. B. Kret and G. R. Madland, "IC Course Part 7: Should you make your own IC's?" The Electronic Engineer, Vol. 25, No. 10, Oct 1966, pp. 75-79.

3. R. L. Hartley and G. R. Madland, "IC Course Part 8: What about linear integrated circuits?", The Electronic Engineer, Vol. 25, No. 10, Oct 1966, p. 87.

4. Donald Christiansen, "Integrated Circuits in Action: Part I, The great design dilemma", Electronics, Vol. 39, No. 21, 17 Oct 1966, pp. 76-78.

5. J. E. Solomon, "Monolithic Analog Circuits", 1967 IEEE International Convention Digest, IEEE, Inc., N. Y., 1967, pp. 370-371.

6. D. P. Schulz and D. J. Dooley, "Integrating space telemetry systems with compatible thin films on silicon", Electronics, Vol. 40, No. 13, 26 Jun 1967, pp. 111-112.

7. Jack Gifford, "The Performance/Economics/Marketplace Interrelationships", Wescon 67 Technical Papers, Wescon, Los Angeles, 1967, p. 4.

8. Donald Christiansen, "Integrated circuits in action: Part II. Trends and trade offs", Electronics, Vol. 39, No. 23, p. 130.

9. National Semiconductor Corporation, Microcircuits Division, A new monolithic operational amplifier design, by R. J. Widlar, Technical Paper TP-2, Santa Clara, Calif., Jun 1967, p. 2.

10. H. C. Lin, et. al., "Advances in Monolithic Integrated Circuits", Semiconductor Products and Solid-State Technology, Vol. 10, No. 4, Apr 1967, pp. 19-20.

11. R. L. Hartley and G. R. Madland, op. cit., p. 82

12. Dwayne King and Lothar Stern, "Designing Monolithic Integrated Circuits", Semiconductor Products and Solid-State Technology, Vol. 8, No. 3, Mar 1965, p. 30.

SECTION 2. CIRCUIT SELECTION

1. Abraham Goodman, "Increasing the Band Range of a Voltage-Controlled Oscillator", Electronic Design, 28 Sep 1964, p. 28.

2. J. H. Kollataj and T. Harkonen, "Integrated circuits in action: part 10. Linearizing sensor signals digitally", Electronics, Vol. 41, No. 5, 4 Mar 1968, pp. 112-113.

3. "Low-cost digital voltmeters", Electro-technology, Vol. 81, No. 1., Jan 1968, p. 67.

4. Hewlett-Packard, Voltage-to-Frequency Converter, Model 2212A, Technical data, 22 Jan 1968, p. 1.

5. Inter-Range Instrumentation Group, Telemetry Standards, Revised Jun 1962, IRIG Document No. 106-60, White Sands Missile Range, New Mexico, Aug 1962, pp. 1,2.

6. BLH Electronics, Inc., SR-4 Foil Gages, FAB Service, Product Data 213, May 1967.

7. W. A. Edson, Vacuum-Tube Oscillators, Wiley and Sons, N. Y., 1953, p. 3.

8. Ibid., p. 265.

9. G. D. Hachtel, "Semiconductor Integrated Oscillators", Ph. D. Thesis, University of California (Berkeley), 1965, pp. 11-15.

10. W. G. Howard and D. O. Pederson, "Integrated Voltage-Controlled Oscillators", Proc. NEC, Vol. 23, 1967, Chicago, Illinois, pp. 279-284.

11. W. A. Edson, op. cit., p. 396.

12. August Hund, "Reactance Tubes in F-M Applications", Electronics, Vol. 15, No. 10, Oct 1942, pp. 68-71, 143.

13. Motorola Semiconductor Products Inc., FM Modulation Capabilities of Epicap VVC's, by Dick Schell, Application Note AN-210, Phoenix, Arizona, 1966, pp. 1-8.

14. W. A. Edson, op. cit., p. 397.

15. J. M. Carroll (ed.), Microelectronic Circuits and Applications, N. Y., McGraw-Hill, 1965, p. 125.

16. Vasil Uzunoglu, "Improving the performance of multipurpose IC's with feedback", Electronics, Vol. 39, No. 13, 27 Jun 1966, pp. 72-73.

17. H. G. Dill, "Semiconductor Inductive Elements", Semiconductor Products, Vol. 5, No. 4, Apr 1962, pp. 30-33.

18. J. M. Carroll, op. cit., pp. 119-121.

19. Jacob Millman and Herbert Taub, Pulse, Digital, and Switching Waveforms, N. Y., McGraw-Hill, 1965, p. 440.

20. W. H. Voelker, "Transistor circuit converts voltage to regulated frequency", Electronics, Vol. 37, No. 29, 16 Nov 1964, pp. 73-74.

21. Maurice Artzt, "Frequency Modulation of Resistance-Capacitance Oscillators", Proc. IRE., Vol. 32, No. 7, Jul 1944, pp. 409-414.

22. M. E. Ames, "Wide-Range Deviable Oscillator", Electronics, Vol. 22, No. 5, May 1949, pp. 96-100.

23. J. M. Sturtevant, "A Voltage-Controlled Multivibrator", Electronics, Vol. 22, No. 10, Oct 1949, pp. 144, 148, 152, 156, 158.

24. L. J. Giacoletto, "Transistorized RC Phase-Shift Power Oscillator", IRE Trans. on Audio, Vol. AU-5, No. 3, May-Jun 1957, pp. 59-62.

25. J. D. Long, "Feedback Linearizes Voltage-to-Frequency Converter", Electronics, Vol. 34, No. 35, 1 Sep 1961, p. 48.

26. R. A. Greiner and S. K. Morgan, "Voltage Controlled Wide-Range Oscillator", Electronics, Vol. 34, No. 51, 22 Dec 1961, pp. 31-35.

27. N. W. Bell and V. Chiunti, "Voltage-Controlled Oscillator Uses Negative Feedback", Electronics, Vol. 35, No. 11, 16 Mar 1962, pp. 64, 65.

28. R. W. Biddlecomb, "Latest Multivibrator Improvement. Linear Voltage-to-Frequency Converter", Electronics, Vol. 36, No. 17, 26 Apr 1963, pp. 64-65.

29. Goodman, op. cit., pp. 28-34.

30. J. R. Giroux, "A wide-range VCO", The Electronic Engineer, Vol. 26, No. 10, Oct 1967, pp. 39-41.

31. Wavetek, Instruction Manual, Models 101, 102, 103, 104, 105, 106, 107, San Diego, Dec 1964, pp. III-5, III-7 to III-17.

32. Dymec, Inc., Handbook for Model DY-2210 Voltage-to-frequency Converter (Serial 186 & above), Palo Alto, Calif., 1959, pp. ii, iii, 3-1 to 3-4.

33. Acromag, Inc., Electronic integrator totalizers, 4-001 Catalog: Section 4, Wixon, Michigan, Sep 1967.

34. Royal Aircraft Establishment, A Voltage Controlled Oscillator for the UK-3 Satellite Telemetry, by W. H. E. Hampton, R. A. E. Technical Report No. 65293, Farnborough, Hants, U. K., Ministry of Aviation, Dec 1965, p. 15.

35. H. C. Lin et al., "Advances in Monolithic Integrated Circuits", Semiconductor Products and Solid State Technology, Vol. 10, No. 4, Apr 1967, pp. 19-20, 23-30.

SECTION 3. CIRCUIT DESIGN

1. E. G. Fubini and M. G. Smith, "Limitations in solid-state technology", IEEE Spectrum, Vol. 4, No. 5, May 1967, pp. 55-59.

2. H. C. Lin et al., "Advances in Monolithic Integrated Circuits", Semiconductor Products and Solid State Technology, Vol. 10, No. 4, Apr 1967, pp. 19-24.

3. R. A. Mammano, "Advances in Linear Monolithic Circuit Technology", Solid State Technology, Vol. 11, No. 3, Mar 1968, p. 32.

4. D. W. Baker and E. A. Herr, "Parasitic Effects in Microelectronic Circuits", IEEE Trans. on Electron Devices, Vol. ED-12, No. 4, Apr 1965, pp. 161-167.

5. Howard Bogert, "Integrated Circuits Can Be Breadboarded", Electronic Design, Vol. 11, No. 4, 15 Feb 1963, pp. 76-78, 80, 82, 83.

6. D. R. Breuer, "Integrated High-Frequency D.C. Amplifiers", Wescon 64 Technical Papers, Wescon, Los Angeles, 1964, pp. 1-9. (Paper 2.2).

7. H. K. Dicken, "Circuit Design Considerations for Integrated Circuits", Semiconductor Products, Jul 1963, pp. 25-30.

8. Hermann Ebenhoech, "Guidelines for the Design of Consumer Linear Integrated Circuits", unpublished paper, Fairchild Semiconductor, Mountain View, Calif., pp. 1-4.

9. Robert Foglesong, "Integrated Circuits Design and Application", Semiconductor Products and Solid State Technology, Vol. 7, No. 3, Mar 1964, pp. 32-34, 39-42.

10. J. W. Gibbs, "Design Considerations in Optimizing Op Amp Cost and Performance", Wescon 67 Technical Papers, Wescon, Los Angeles, 1967, pp. 1-5. (Paper 1/3, Part 1).

11. Jack Gifford, "The Performance/Economics/Marketplace Inter-Relationships", Wescon 67 Technical Papers, Wescon, Los Angeles,1967, pp. 1-8. (Paper 1/3, Part 2).

12. J. R. Hulme, "Design Considerations for Solid State Integrated Circuits", Solid State Design, Vol. 4, No. 7, Jul 1963, pp. 33-38.

13. Dwayne King and Lothar Stern, "Designing Monolithic Integrated Circuits", Semiconductor Products and Solid State Technology, Vol. 8, No. 3, Mar 1965, pp. 21-32.

14. H. C. Lin, "Diode Operation of a Transistor in Functional Blocks", IEEE Trans. on Electron Devices, Vol. ED-10, No. 3, May 1963, pp. 189-194.

15. H. C. Lin, "Design Considerations for Linear Functional Blocks", Solid State Design, Vol. 5, No. 7, Jul 1964, pp. 44-49.

16. H. C. Lin et al., "Lateral Complementary Transistor Structure for the Simultaneous Fabrication of Functional Blocks", Proc. IEEE, Vol. 52, No. 12, Dec 1964, pp. 1491-1495.

17. Motorola Inc., Semiconductor Products Division, Engineering Staff, Integrated Circuits Design Principles and Fabrication, by R. M. Warner et al. (eds.), N. Y., McGraw-Hill, 1965, pp. 66, 67, 127-165, 174-207, 255-264.

18. Motorola Inc., Semiconductor Products Division, Engineering Staff, Analysis and Design of Integrated Circuits, by D. K. Lynn, C. S. Meyer, and D. J. Hamilton (eds.), N. Y., McGraw-Hill, 1967, pp. 31-33.

19. R. J. Widlar, "A Monolithic High Gain D-C Amplifier", Proc. NEC, Vol. 20, Oct 1964, pp. 169-174.

20. R. J. Widlar, "A Unique Circuit Design for a High Performance Operational Amplifier Especially Suited to Monolithic Construction", Proc. NEC, Vol. 21, Oct 1965, pp. 85-89.

21. R. J. Widlar, "Some Circuit Design Techniques for Linear Integrated Circuits", IEEE Trans. on Circuit Theory, Vol. CT-12, No. 4, Dec 1965, pp. 586-590.

22. R. J. Widlar, "An Exact Expression for the Thermal Variation of the Emitter Base Voltage of Bi-Polar Transistors", Proc. IEEE, Vol. 55, No. 1, Jan 1967, pp. 96-97.

23. National Semiconductor Corporation, A Versatile, Monolithic Voltage Regulator, by R. J. Widlar, AN-1, Santa Clara, Calif., Nov 1967.

24. Mark Weissenstern and Robert Beeson, "Constraints in Designing Integrated Circuits", Electronic Design, Vol. 11, No. 4, 15 Feb 1963, pp. 66-68, 70-75.

25. Vasil Uzunoglu, "Considerations in the Utilization of Semiconductor Devices and Integrated Circuits", Semiconductor Products and Solid State Technology, Vol. 10, No. 3, Mar 1967, pp. 29, 30, 35-40.

26. General Instrument Corp., Microelectronics Division, Criteria for Designing Custom MTOS LSI Circuits, by Lester Penner, Hicksville, N. Y., Oct 1967, pp. 1-7.

27. Crystalonics, A Designer's Guide to Crystalonics Hybrid Microcircuits, Cambridge, Mass., p. 4 (undated product brochure).

28. Motorola Inc., Semiconductor Products Division, Engineering Staff, Analysis and Design & Integrated Circuits, op. cit., pp. 103-131.

29. Paul M. Chirlian, Integrated and Active Network Analysis and Synthesis, Englewood Cliffs, N. J., Prentice-Hall, 1967, pp. 131, 234, 315.

30. Motorola Inc., Semiconductor Products Division, Engineering Staff, Analysis and Design of Integrated Circuits, op. cit., pp. 111-116, 127-129.

31. J. J. Sparkes, "Device Modeling", IEEE Trans. on Electron Devices, Vol. ED-14, No. 5, May 1967, p. 229.

32. Fubini and Smith, loc. cit.

33. H. C. Lin et. al., "Advances in Monolithic Integrated Circuits", Semiconductor Products and Solid-State Technology, Vol. 10, No. 4, Apr 1967, p. 24.

34. Hermann Ebenhoech, op. cit., p. 2.

35. Motorola Semiconductor Products Inc., Useful Frequency Range Extension for MC1530 Operational Amplifiers, by L. L. Wisseman, AN-276, Phoenix, Arizona, 1966, p. 2.

36. R. A. Mammano, loc. cit.

37. Konrad Weniger, "Gain-bandwidth Chart on Linear IC's", The Electronic Engineer, Vol. 26, No. 6, Jun 1967, p. 114.

38. C. V. Weden, "Operational Amplifier Principles", Analog Dialogue, Vol. 1, No. 2, Cambridge, Mass., Analog Devices, Inc., Jun 1967, p. 10.

39. Analog Devices, Inc., Operational Amplifiers, Part I - Principles of Operation and Analysis of Errors, by Roy Stata, Cambridge, Mass. (undated).

40. Analog Devices, Inc., Operational Amplifiers, Part II - Inverting, non-inverting, and Differential Configurations, by Roy Stata, Cambridge, Mass. (undated).

41. Analog Devices, Inc., Operational Amplifiers, Part IV - Offset and Drift in Operational Amplifiers, by Roy Stata, Cambridge, Mass. (undated).

42. Burr-Brown Research Corp., Handbook of Operational Amplifier Applications, Tucson, Arizona, 1963, pp. 1-44.

43. Burr-Brown Research Corporation, Handbook of Operational Amplifier Active RC Networks, Second Edition, Tucson, Arizona, 1966, pp. 15-26.

44. Fairchild Semiconductor, Fairchild Semiconductor Linear Integrated Circuits Applications Handbook, by J. N. Giles (ed.), Mountain View, Calif., 1967, pp. 17-25.

45. Radio Corporation of America, RCA Linear Integrated Circuit Fundamentals, Harrison, J. J., 1966, pp. 62-86.

46. Burr-Brown Research Corporation, Handbook of Operational Amplifier Applications, op. cit., pp. 21, 23.

47. Fairchild Semiconductor, op. cit., p. 27.

48. Radio Corporation of America, op. cit., p. 9.

49. R. D. Middlebrook, Differential Amplifiers, N. Y., Wiley and Sons, 1963, pp. 4-75.

50. Radio Corporation of America, op. cit., pp. 8-59.

51. Middlebrook, op. cit., pp. 45-47.

52. Radio Corporation of America, op. cit., pp. 13-14.

53. Motorola Semiconductor Products Inc., High Performance Integrated Operational Amplifiers, by Leo Wisseman and J. J. Robertson, AN-204, Phoenix, Arizona, 1966, pp. 3,4.

54. H. Abraham and E. Bloch, Annal. d. Phys., Vol. 12, Sep-Oct 1919, p. 237, cited by E. R. Shenk, "The Multivibrator: Applied Theory and Design, Part III," Electronics, Vol. 17, No. 3, Mar 1944, p. 154.

55. Jacob Millman and Herbert Taub, Pulse, Digital, and Switching Waveforms, N. Y., McGraw-Hill, 1965, pp. 437-441.

56. Ibid., p. 891.

57. Abraham Goodman, "Increasing the Band Range of a Voltage-Controlled Oscillator," Electronic Design, 28 Sep 1964, p. 30.

58. Weden, loc. cit.

59. Ray Stata, "Operational Integrators", Analog Dialogue, Vol. 1, No. 1, Cambridge, Mass., Analog Devices, Inc., Apr 1967, pp. 6-9.

60. Motorola Semiconductor Products Inc., Useful Frequency Range Extension for MC1530 Operational Amplifiers, loc. cit.

61. Ibid.

62. Fairchild Semiconductor, op. cit., pp. 65-68.

63. Fairchild Semiconductor, Frequency Compensation Techniques for an Integrated Operational Amplifier, by J. N. Giles, Application Bulletin APP-117/2, Mountain View, Calif., Feb. 1966, pp. 1-8.

64. Radio Corporation of America, op. cit., pp. 78-94.

65. Fairchild Semiconductor, Frequency Compensation Techniques for an Integrated Operational Amplifier, op. cit., p. 2.

66. Motorola Semiconductor Products Inc., High Performance Integrated Operational Amplifiers, op. cit., p. 7.

SECTION 4. CIRCUIT EVALUATION

1. Dwayne King and Lothar Stern, "Designing Monolithic Integrated Circuits," Semiconductor Products and Solid State Technology, Vol. 8, No. 3, Mar 1965, p. 32.

2. E. G. Fubini and M. G. Smith, "Limitations in Solid-State Technology", IEEE Spectrum, Vol. 4, No. 5, May 1967, p. 59.

3. Howard Bogert, "Integrated Circuits Can Be Breadboarded", Electronic Design, Vol. 11, No 4, 15 Feb 1963, p. 76.

4. J. R. Hulme, "Design Considerations for Solid State Integrated Circuits", Solid State Design, Jul 1963, pp. 33, 35.

5. King and Stern, op. cit., pp. 31-32.

6. Motorola Semiconductor Products Inc., Technical Staff, "Designing Digital Monolithic Integrated Circuits," Microelectronics and Reliability, Vol. 4, No. 4, Dec 1965, pp. 340, 343.

7. Mark Weissenstern and Robert Beeson, "Constraints in Designing Integrated Circuits," Electronic Design, Vol. 11, No. 4, 15 Feb 1963, p. 75.

8. Jerome Eimbinder, "General-purpose IC Chips Speed Analog Design Work", Electronics, Vol. 39, No. 6, 21 Mar 1966, pp. 88, 89.

9. Hulme, op. cit., p. 36.

10. King and Stern, loc. cit.

11. Fairchild Semiconductor, Fairchild Semiconductor Linear Integrated Circuits Applications Handbook, by J. N. Giles (ed.), Mountain View, Calif., 1967, p. 52.

12. Ibid., p. 53.

13. Ibid., p. 136.

14. Burr-Brown Research Corp., Handbook of Operational Amplifier Applications, Tucson, Arizona, 1963, pp. 74-79.

15. Analog Devices, Inc., A Comprehensive Catalog and Guide to Operational Amplifiers, Cambridge, Mass., pp. 11-17. (undated).

16. D. W. Baker and E. A. Herr, "Parasitic Effects in Microelectronic Circuits," IEEE Trans. on Electron Devices, Vol. ED-12, No. 4, Apr 1965, pp. 166-167.

17. Hermann Ebenhoech, "Guidelines for the Design of Consumer Linear Integrated Circuits," Unpublished paper, Fairchild Semiconductor, Mountain View, Calif., pp. 1-4.

18. Hulme, op. cit., pp. 34, 36.

19. Integrated Circuit Engineering Corp., Integrated Circuit Engineering, by G. R. Madland, et. al., Fourth Edition, Cambridge, Mass., Boston Technical Publishers, Inc., 1966, pp. 291-309.

20. Motorola Inc., Semiconductor Products Division, Engineering Staff, Integrated Circuits Design Principles and Fabrication, by R. M. Warner et. al. (eds.), N. Y., McGraw-Hill, 1965, pp. 156-165, 177-178, 261.

21. Motorola Inc., Semiconductor Products Division, Engineering Staff, Analysis and Design of Integrated Circuits, by D. K. Lynn, C. S. Meyer, and D. J. Hamilton (eds.), N. Y., McGraw-Hill, 1967, pp. 17, 34, 414.

22. J. E. Solomon and T. M. Frederiksen, "Monolithic Analog Circuits", 1967 IEEE International Convention Digest, IEEE, Inc., N. Y., 1967, p. 371.

23. Edward Keonjian (ed.), Microelectronics, N. Y., McGraw-Hill, 1963, p. 312.

24. Integrated Circuits Engineering Corp., op. cit., p. 302.

SECTION 5. SUMMARY AND CONCLUSIONS

1. Fairchild Semiconductor, Fairchild Semiconductor Linear Integrated Circuits Applications Handbook, by J. N. Giles (ed.), Mountain View, Calif., 1967, p. 57.

2. Fairchild Semiconductor, OEM Price List, Mountain View, Calif., 1 May 1968, p. OEM-15.

APPENDIX I. GLOSSARY

1. J. B. Brauer and E. P. O'Connell, "Microelectronics -Where, Why, and When?", Electronic Industries, Vol. 23, No. 9, Sep 1964, p. 32.

2. Donald Christiansen, "Integrated Circuits in Action: Part I. The Great Design Dilemma", Electronics, Vol. 39, No. 21, 17 Oct 1966, p. 83.

3. Donald Christiansen, "Integrated Circuits in Action: Part II. Trends and Trade-Offs", Electronics, 14 Nov. 1966, Vol. 39, No. 23, 14 Nov 1966, p. 132.

4. Motorola Inc., Semiconductor Products Division, Engineering Staff, Integrated Circuits Design Principles and Fabrication, by R. M. Warner et al. (eds), N. Y., McGraw-Hill, 1965, pp. xxi-xxii.

5. IEEE, Standard Definitions of Terms for Integrated Electronics, IEEE Standard No. 274, N. Y , Dec 1966.

6. Adi J. Khambata, Introduction to Integrated Semiconductor Circuits, Wiley and Sons, N. Y., 1963, pp. 7-9.

7. Dwayne King and Lothar Stern, "Designing Monolithic Integrated Circuits", Semiconductor Products and Solid State Technology, Vol. 8, No. 3, Mar 1965, pp. 21-22.

8. D. B. Kret, D. Thompson, and F. H. Bower, "Integrated Circuits Course. Part 2: Removing the Mystery From IC Processing", The Electronic Engineer, Vol. 25, No 8, Aug 1966, pp. 97, 100, 101.

9. J. W. Lathrop, "Semiconductor-Network Technology--1964", Proc. IEEE, Vol. 52, No. 12, Dec 1964, pp. 1430-1437, 1440-1443.

10. G. R. Madland and J. Jolly, "Integrated Circuits Course. Part 1: The Importance of Integrated Circuits Yield to Engineers", The Electronic Engineer, Vol. 25, No. 8, Aug 1966, p. 88.

11. W. E. Montgomery et al., "Application of Integrated Electronics to Military Communications and Radar Systems", Proc. IEEE, Vol. 52, No. 12, Dec 1964, pp. 1721-1722.

12. W. A. Notz et. al., "Benefitting the Systems Designer," Electronics, Vol. 40, No. 4, 20 Feb 1967, p. 130.

13. Sandia Corp., Microelectronics: Solid State and Thin Film Advanced Development, by N. J. Pollard et. al., Sandia Corp. Reprint SC-R-64-1360, Albuquerque, New Mexico, Feb 1965, pp. 5-10.

14. H. K. Dicken and D. B. Kret, "IC Course Part 6. Assembling Integrated Circuits", The Electronic Engineer, Vol. 25, No. 10, Oct 1966, pp. 66-67.

15. H. C. Lin et. al., "Advances in Monolithic Integrated Circuits", Semiconductor Products and Solid-State Technology, Vol. 10, No. 4, Apr. 1967, p. 24.

16. Radiation Inc., Microelectronics Division, All Products Bulletin, Melbourne, Florida, Jul 1967, p. 2.

17. M. P. Lepselter et. al., "Beam-Lead Devices and Integrated Circuits", Proc. IEEE, Vol. 53, No. 4, Apr 1965, p. 405.

18. M. P. Lepselter, "Beam-Lead Sealed-Junction Technology", Bell Laboratories Record, Vol. 44, No. 9, Oct-Nov 1966, pp. 298-303.

19. M. P. Lepselter, "Beam-Lead Technology", The Bell System Technical Journal, Vol. 45, No. 2, Feb 1966, pp. 233-253.

20. "LSI, Fairchild Style", Electronics, Vol. 41, No. 3, 5 Feb 1968, p. 45.

21. H. C. Lin et. al., "Lateral Complimentary Transistor Structure for the Simultaneous Fabrication of Functional Blocks", Proc. IEEE, Vol. 52, No. 12, Dec 1964, pp. 1491-1492.

22. H. C. Lin et. al., "Advances in Monolithic Integrated Circuits", op. cit., pp. 25, 26, 28.

23. D. B. Kret, D. Thompson, and F. H. Bower, op. cit., p. 100.

24. IEEE, loc. cit.

25. E. Keonjian (ed.), Micropower Electronics, N. Y., MacMillan, 1964, 216 pp.

26. Motorola Inc., Semiconductor Products Division, Engineering Staff, op. cit., p. xxi.

27. H. K. Dicken, "Circuit Design Considerations for Integrated Circuits", Semiconductor Products, Vol. 6, No. 7, Jul 1963, p. 25.

28. J. E. Thomas Jr., "Materials Problems in Integrated Circuits", 1967 IEEE International Convention Digest, N. Y. IEEE, 1967, pp. 298-299.

29. J. M. Carroll (ed.), Microelectronics Circuits and Applications, N. Y., Mc Graw-Hill, 1965, p. 12.

30. Adi J. Khambata, op. cit., p. 25.

31. Fairchild Semiconductor, Fairchild Semiconductor Linear Integrated Circuits Applications Handbook, by J. N. Giles (ed.), Mountain View, Calif., 1967, p. 1.

32. National Semiconductor Corp., Microcircuits Division, A New Monolithic Operational Amplifier Design, by R. J. Widlar, Technical Paper TP-2, Santa Clara, Calif., Jun 1967, p. 2.

33. H. C. Lin et. al., "Advances in Monolithic Integrated Circuits", op. cit., pp. 19,20.

34. J. B. Brauer and E. P. O'Connell, op. cit., p. 36.

35. J. W. Lathrop, op. cit., p. 1441.

36. F. P. Heiman, "The Future Role of Field-Effect Devices in Electronics", 1967 IEEE International Convention Digest, N. Y., IEEE, 1967, p. 120.

37. J. W. Lathrop, op. cit., p. 1440.

38. R. J. Widlar, "A Unique Circuit Design for a High Performance Operational Amplifier Especially Suited to Monolithic Construction", Proc. NEC, Vol. 21, Chicago, Illinois, Oct 1965, p. 86.

39. D. B. Kret, D. Thompson, and F. H. Bower, op. cit., p. 97.

APPENDIX II. THE MONOLITHIC IC.

1. J. B. Brauer and E. P. O'Connell, "Microelectronics -- Where, Why, and When?", Electronic Industries, Vol. 23, No. 9, Sep 1964, p. 36.

2. P. E. Haggerty, "Integrated Electronics--A Perspective", Proc. IEEE, Vol. 52, No. 12, Dec 1964, pp. 1440-1495.

3. J. M. Carroll (ed.), Microelectronic Circuits and Applications, N. Y., McGraw-Hill, 1965, pp. 3, 12.

4. J. M. Bridges, "Integrated Electronics in Defense Systems," Proc. IEEE, Vol. 52, No. 12, Dec 1964, pp. 1406-1407.

5. J. M. Carroll, op. cit., p. 17.

6. Robert Noyce, "Turning a Science into an Industry", IEEE Spectrum, Vol. 3, No. 1, Jan 1966, p. 99. (Interview by Nilo Lindgren).

7. "Electronic Markets 1968", Electronics, Vol. 41, No. 1, 8 Jan 1968, pp. 109-110.

8. P. E. Haggerty, "Integrated Electronics--A Perspective", Proc. IEEE, Vol. 52, No. 12, Dec 1964, p. 1402.

9. E. F. Kvamme, "Integrated Circuits--Their Current Technical and Economic Status", 1967 IEEE International Convention Digest, N. Y., IEEE, 1967, p. 369.

10. Fairchild Semiconductor, Designing with Off-the-Shelf Linear Microcircuits, by R. J. Widlar and J. N. Giles, Application Bulletin APP-124, Mountain View, Calif., Jan 1966, p. 1.

11. Robert Noyce, op. cit., p. 100.

12. G. R. Madland, "Looking under the Hood", Electronic Products, Vol. 9, No. 1, Jun 1966, p. 9.

13. F. H. Bower and H. K. Dicken, "Integrated Circuits Course Part 3: Photo Masks ... The Tooling for ICs", The Electronic Engineer, Vol. 25, No. 8, Aug 1966, pp. 103-113.

14. J. M. Carroll, op. cit., pp. 12-14, 16.

15. Fairchild Semiconductor, Fairchild Semiconductor Linear Integrated Circuits Application Handbook, by J. N. Giles (ed.), Mountain View, Calif., 1967, pp. 1-8.

16. J. W. Lathrop, "Semiconductor-Network Technology -- 1964", Proc. IEEE, Vol. 52, No. 12, Dec 1964, pp. 1430-1444.

17. H. C. Lin et. al., "Advances in Monolithic Integrated Circuits", Semiconductor Products and Solid-State Technology, Vol. 10, No. 4, Apr 1967, pp. 19-30.

18. Motorola Inc., Semiconductor Products Division, Engineering Staff, Integrated Circuits Design Principles and Fabrication, by R. M. Warner et. al. (eds.), N. Y., McGraw-Hill, 1967, pp. 130-165, 174-207, 255-264, 273-286.

19. H. C. Lin, "Diode Operation of a Transistor in Functional Blocks", IEEE Trans. on Electron Devices, Vol. ED-10, No. 3, May 1963, pp. 189-194.

20. H. C. Lin et. al., "Lateral Complementary Transistor Structure for the Simultaneous Fabrication of Functional Blocks", Proc. IEEE, Vol. 52, No. 12, Dec 1964, pp. 1491-1495.

21. Hermann Ebenhoech, "Guidelines for the Design of Consumer Linear Integrated Circuits", unpublished paper, Fairchild Semiconductor, Mountain View, Calif., p. 2.

22. W. E. Montgomery et. al., "Application of Integrated Electronics to Military Communications and Radar Systems", Proc. IEEE, Vol. 52, No. 12, Dec 1964, p. 1722.

23. D. W. Baker and E. A. Herr, "Parasitic Effects in Microelectronic Circuits", IEEE Trans. on Electron Devices, Vol. ED-12, No. 4, Apr 1965, pp. 162-165.

24. R. A. Mammano, "Advances in Linear Monolithic Circuit Technology", Solid State Technology, Vol. 11, No. 3, Mar 1968, p. 32.

25. H. C. Lin et. al., "Advances in Monolithic Integrated Circuits", op. cit., p. 24.

26. Donald Christiansen, "Integrated Circuits in Action: Part 1. The great design dilemma", Electronics, Vol. 39, No. 21, 17 Oct 1966, p. 78.

27. G. R. Madland, "Madland Evaluates Signetics Corp.", Electronic Products, Jul 1967, p. 10.

28. G. R. Madland, "Quick rise time in linears. Glen Madland evaluates RCA's IC capabilities", Electronic Products, Nov 1967, p. 12.

29. Navy Underwater Sound Laboratory, High Performance Microelectronic Amplifiers for Deep Submergence Applications, by J. J. Libuha and J. H. Mascarenhas, Report No. 844, New London, Connecticut, 25 Oct 1967, pp. 1-4.

30. Fairchild Semiconductor, "Designing with Off-the-Shelf Linear Microcircuits", loc. cit.

APPENDIX I

GLOSSARY

In considering a device as new as the IC, terminology is often confusing, and definitions are sometimes arbitrary. The definitions provided below apply in this paper, and most have fairly wide acceptance.[1-13] Terms which are sometimes considered synonyms, but which are not used in this paper, are given in parenthesis following defined entries.

Analog IC. See linear IC.

Buried Layer. The n+ region, which is formed by diffusion into the p-type substrate, prior to growing the n-type epitaxial layer, during the standard six-mask monolithic IC fabrication. Reasons for its presence are given in Appendix II.

Chip. A small piece of semiconductor material, containing a single device. If the device is a monolithic IC, then "chip" is synonymous with "die".

Compatible. Any element, other than the standard resistors, diodes, and npn transistors, which can be formed during the six-mask monolithic IC fabrication without requiring any additional (and thus costly) steps. For example, we speak of the compatible lateral pnp transistor, and the compatible MOS capacitor.

Compatible monolithic IC. See hybrid IC.

Dice. In monolithic IC fabrication, the square or rectangular pieces of the wafer. Each die contains a single IC. Dice range from 20 mils square to about 80 mils by 200 mils. Typically, the wafer is first scribed, then broken into dice between rubber rollers.[14]

Diffusion. In monolithic IC fabrication, the substition of donor (n-type, valence 5) or acceptor (p-type, valence 3) impurity atoms for silicon atoms within the crystal lattice. This is accomplished by exposure of the wafer to the desired impurity atoms at elevated temperatures (on the order of 1100° C), and is controlled by regulating time, temperature, and the amount of impurity atoms present.

Digital IC. An IC which is designed to handle only discrete signals, such as binary pulse trains. A digital IC may be composed of linear as well as non-linear elements. IC's are either digital or linear.

Epitaxial growth. In IC fabrication, the forming of an intrinsic or extrinsic semiconductor layer on the surface of the wafer, so that the layer consists of an exact extension of the monocrystalline wafer structure. Both the epitaxial layer and the wafer are generally, but not necessarily, extrinsic Silicon. Epitaxial growth is accomplished in a suitable environment at elevated temperatures.

Film IC. The general class of IC's which includes both thin film and thick film IC's.

Fully-integrated electronics. See monolithic IC.

Functional block. See monolithic IC.

Functional electronic block. See monolithic IC.

Hybrid IC. A combination of monolithic and film techniques. There are two common hybrid IC types today: the device (monobrid IC, multichip IC) formed by the addition of Si chips, containing monolithic IC's or single active devices, to a film IC; and the device (compatible monolithic IC) where thin film passive components are deposited onto a monolithic IC.

Integrated circuit. (Microcircuit, microstructure). Abbreviated "IC". A device consisting of two or more inseparable elements, mounted on or within a common substrate, and connected together to form a single electrical network.

Integrated electronics. See microelectronics.

Isolation. The electrical separation of components. In IC's, reverse-biased pn junction, resistive, dielectric, and physical isolation are used; the first is the most common,[15] and dominates monolithic IC production. However, Radiation, Inc. claims to have made dielectric isolation competitive with diode isolation,[16] and Bell Telephone Laboratories reports much progress in perfecting its technique of "beam-lead" isolation, a form of physical isolation.[17-19]

Kit parts. The trade name given by Fairchild Semiconductor to monolithic IC elements (e.g., IC transistor pairs in TO-5 cans) utilized in breadboarding IC's.

Large scale integration. Abbreviated "LSI". No standard definition, but generally considered to indicate complexity of over 100 components on the order of gates per chip.[20] "MSI" has been coined to indicate component densities somewhere between the rather arbitrary "standard" IC's and the equally arbitrary LSI.

Lateral pnp transistor. In monolithic IC fabrication, the compatible pnp transistor typically formed by concentric p-type diffused regions separated by the n-type epitaxial layer.[21] Performance of the lateral pnp transistor is limted by its comparitively wide base, which in turn is limited by mask resolution to about 0.5 mils minimum width.[21,22]

Linear IC. (Analog IC). An IC designed to handle either continuous signals, or a combination of continuous and discrete signals. A comparator is an example of the latter,as is the VCO discussed in this paper. Linear IC's may contain both linear and nonlinear elements. All IC's are either linear or digital.

Medium scale integration. Abbreviated "MSI". See large scale integration.

Metallization. In monolithic IC fabrication, the depositing by vacuum evaporation of a metal film on the oxide-coated wafer, to provide contacts, interconnections, and MOS capacitor plates. Aluminum is the most common metal used.[23]

Microcircuit. See IC.

Microelectronics. (Integrated electronics). The entire class of circuits which have component densities higher than can be achieved with convenient methods and discrete components. Microelectronics is subdivided into monolithic IC's, film IC's, hybrid IC's, and molecular electronics. The IEEE prefers "Integrated Electronics" to "Microelectronics", feeling that the latter places undue emphasis on size, while the former more correctly stresses the significance of interconnections.[24]

Micropower electronics. The general area of minimizing power levels required in electronic devices. Although this was fairly important prior to IC's, the greatly increased component densities attained in IC's have made micropower an essential criterion in circuit design.[25]

Microstructure. See IC.

Molecular IC. See IC.

Molecular electronics. (Morphological electronics). A class of microelectronics, still largely in the research stage, which consists of devices wherein it is impossible to isolate and identify functional elements. As an example, some writers have classified the piezoelectric crystal as a molecular IC.[26]

Monobrid IC. See hybrid IC.

Monolithic IC. (Fully-integrated electronics, functional block, functional electronic block, molecular IC, semiconductor IC, solid-state IC). A device wherein active and passive elements and the substrate are formed from the same piece of semiconductor material, usually monocrystalline silicon. Silicon is usually used because of its wide temperature range, and to exploit the natural passivating property of SiO_2, which is easily formed and which is compatible with existing photographic processes.[27-29]

Morphological electronics. See molecular electronics.

Multichip IC. See hybrid IC.

Planar process. A technique of surface passivation, i.e., isolation of the surface of a semiconductor device from its environment by the fabrication of a suitable insulating layer on that surface.[30] In monolithic IC fabrication, surface passivation is achieved by a silicon dioxide layer as described in Appendix II. Planar is a patented Fairchild process.[31]

Semiconductor IC. See monolithic IC.

Six-mask fabrication process.* The standard planar-epitaxial process of fabricating monolithic IC's with buried n+ regions. The six-mask process currently dominates monolithic fabrication, due to its decided cost advantage;[32-33] it is described in some detail in Appendix II.

Solid-state IC. See monolithic IC.

---

*The term "six mask process" was apparently coined by Widlar, Ref. 32.

Substrate. Literally, foundation In monolithic IC fabrication, the original silicon wafer, usually p-type, on and in which the IC is formed.

Thick film IC. A device similar to thin film IC's. "Thick" is supposed to indicate visible thickness, which must be on the order of 10-100 microns; however, "thick" is generally used to indicate films formed by other than vacuum evaporation. Thick films have been in use for many years, and are usually made by silk-screening.[34-35]

Thin-film IC. A device whose passive elements and interconnections are formed from thin (typically less than 1 micron) films of various materials, which have been deposited on a passive substrate by methods such as vacuum evaporation. Thin film active elements are presently impractical for mass production IC's;[36] true thin film IC's are only passive. Thin-film technology is sometimes referred to as "vacuum technology", which is a slightly more restrictive term.[37]

Vertical pnp transistor. In monolithic IC fabrication, the compatible pnp transistor formed so that its emitter, base and collector are essentially oriented vertically with respect to each other. This orientation requires that the substrate be used for the collector. Typically, the npn base and collector diffusions form the vertical pnp emitter and base respectively. Current gain is normally higher than for the lateral pnp transistor.[38]

Wafer. In monolithic IC fabrication, the thin, roughly circular slices of the original single Si crystal. Thickness is typically

6 mils. Diameter depends directly, of course, on the diameter of the crystal; diameters are on the order of an inch or two.[39]

Yield. In monolithic IC production, the percentage of usable IC's which remain from the total number formed on the wafer, after fabrication and packaging.

APPENDIX II

THE MONOLITHIC IC

1. An Overview

Electronics traditionally has been a series of compromises between the diverging requirements of reliability, performance, cost, and size. However, one new device, the integrated circuit, has created the unique situation of simultaneous increase in reliability and performance, and decreases in size and cost.[1]

The development in 1958, by Jack S. Kilby of Texas Instruments, Inc., of a rudimentary monolithic IC, is generally considered to mark the inception of true integration.[2] It should be noted, however, that this work was under contract from the U. S. Air Force's Aeronautical Systems Division at Wright-Patterson Air Force Base, Dayton, Ohio; the ASD has formulated the monolithic IC concept as early as 1953.[3] In fact, the Department of Defense provided much of the momentum for integrated circuit development; and, in addition, was the largest market for IC's in their early years.[4,5] It was not until 1965 that the commercial unit sales volume became equal to that of the military.[6]

Digital IC's have accounted for most IC sales to date.[7] Digital function requirements are few and standard; these were readily duplicated by monolithic IC's. Once early problems with parasitic collector-substrate capacitance and large collector bulk resistance were resolved, digital IC's offered comparable performance to equivalent discrete circuits,[8] at lower cost. Acceptance of IC's for digital requirements has increased so much that today virtually every new computer being built uses digital IC's.[9]

Linear IC's have not progressed as well as digital ones. There are almost limitless varieties of different linear applications which might be realized as linear IC's; however, most of these are so specialized as to have low potential sales, and thus are not good IC prospects. Instead, IC manufacturers have produced mainly general-purpose linear IC's, and advocated using these with suitable external components to realize desired responses.[10] This suggestion has met with less than extreme enthusiasum from the rest of the electronics industry. Moreover, current limitations in the dominant monolithic technology have restricted realization of many circuit requirements, such as broad bandwidths or sharp tuning, in the linear domain.[11]

The monolithic IC today is at a threshold between generations. The digital monolithic IC appears to be on the verge of an irreversible step into LSI. Where the linear monolithic IC is heading is not so clear. Possibly, improvements in technology will permit realization of the circuit functions that are so elusive today. And, in any case, hopefully, application of suitable design methods to realistic objectives will result in linear IC's that will find wider acceptance in tomorrow's market place.

Monolithic IC's are evolutionary, rather than revolutionary, devices; their technology is merely an extension of the previous transistor techniques. Because of this evolutionary nature, the misconception might arise that monolithic IC's are easy to design, or at least to evaluate. Unlike other electronic components, however, even proper evaluation of monolithic IC's requires some knowledge of their fabrication. At least one IC expert recommends that potential

users compare monolithic IC manufacturers by microscopic examination of their products;[12] this certainly requires greater intimacy with component technology than was ever required of transistor users. This brings us back to the mutual education problem, discussed in the Introduction: the fabrication information in the next section is certainly an essential part of the education of the potential monolithic IC user.

2. Fabrication: The Six-Mask Method

This section contains a description of one method of making monolithic IC's.* As pointed out in the introduction, the monolithic Si IC represents the dominant technology today. The prevalent methods of monolithic Si IC production usually involve five or six masks; the sixth mask is required when a buried n+ region is needed.

We first consider some aspects of the photomasking-etching and diffusion procedures, since these are repeated several times during fabrication. Then the six major process steps are covered; included here are the reasons for having the buried n+ region. Fabrication parameters are mainly controlled by the type of npn transistor desired in the IC; it is appropriate then that we use a single npn transistor to illustrate photomasking-etching, diffusion, and the fabrication methodology.

Our integrated VFC requires other components in addition to npn transistors; the methods of deriving these components from the basic

*Information here is mainly a condensation and correlation of several sources.[13-18] Several examples in this section involve specific numbers, which represent "typical" values as reflected in these sources.

npn processes are discussed next. We also discuss the reasons for capacitors being difficult to fabricate, and inductors impossible.

Next, we briefly examine the standard monolithic isolation method: the back-biased pn diode.

Finally we consider cost aspects of monolithic IC fabrication; these in turn dictate a rough set of monolithic IC design guidelines.

Photomasking and Etching

The microscopic dimensions of the monolithic IC are the source of many of its advantages and its problems. The key to achieving these microscopic dimensions predictably, while simultaneously fabricating many IC's, is selective etching to remove unwanted material. This etching is controlled by photolithography. First, the wafer surface is covered with a thin (6μ) photo-resist emulsion. Then the emulsion is exposed to high intensity ultraviolet light through a photo mask. The mask, created from precise artwork by equally precise microphotography, is the tooling of the IC industry; by determining what areas of the photo-resist are illuminated by the ultraviolet light, the mask ultimately determines where etching and subsequent diffusion or connections will occur.

The photo-resist is polymerized in the exposed areas. Developing removes the photo-resist in the unexposed areas. Then the wafer is subjected to a hydrofluoric acid etch. The polymerized photo-resist is acid resistant, so the etch only removes material from the wafer surface where no photo-resist remains; i.e., areas of the surface which were covered by opaque regions of the mask and hence were not exposed to ultra-violet light.

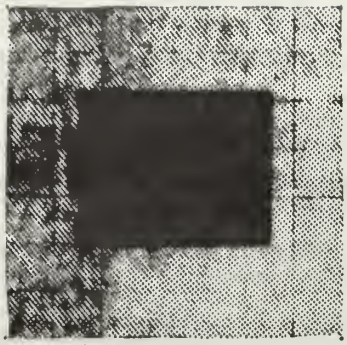
Photomasking and etching is used to form "windows" in the protective layer of silicon dioxide which covers the wafer surface; these windows permit diffusion in selected regions, and also provide access to the semiconductor portion of the wafer. In addition, this technique is used to remove excess metallization in forming the contacts and interconnections.

In the six-mask method, the following masks are required:

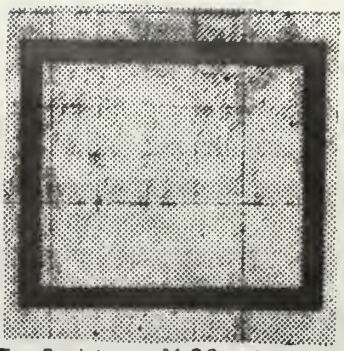
1. Pre-epi diffusion (buried n+ layer).
2. Isolation diffusion.
3. Base diffusion.
4. Emitter diffusion.
5. Contact holes.
6. Metallization.

Examples of the masks are shown in Figure II-1 for an illustrative transistor. This is obviously only a tutorial transistor, since the leads are not connected to anything, and are too small for bonding to the 1 mil wires typically used for connections off the chip. Note that the opaque regions on the masks, as explained above, correspond to regions on the chip where undesired material is to be removed.

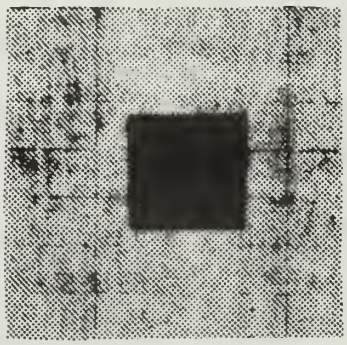
It is important to keep in mind that the masks are the only control over location of IC elements, and are the primary control over the elements' lateral dimensions. These lateral dimensions are on the order of mils; line widths of .2 mils (5μ) and tolerances of .05 mils (1.25μ) are common.



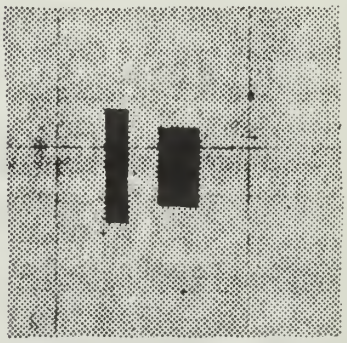
(a). Pre-epi diffusion (n+) mask.



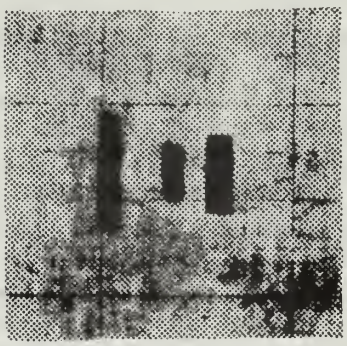
(b). Isolation diffusion (p+) mask.



(c). Base diffusion (p) mask.

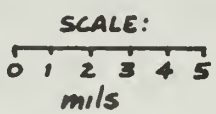


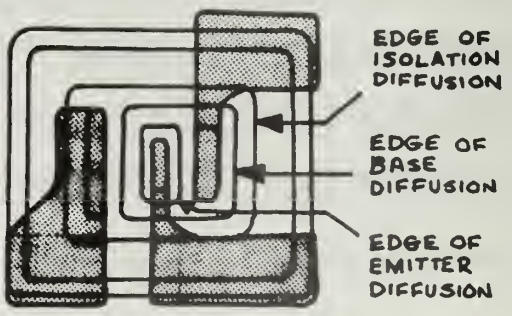
(d). Emitter diffusion (n+) mask.



(e). Contact holes mask.

(f). Metallization mask.





(g). Sketch of completed transistor (shaded areas are metallization).

Figure II-1: A mask set example.

Diffusion

Like the photomasking/etching process, diffusion is a repeated step in the batch fabrication of monolithic IC's. The preceding section mentioned the four diffusions which are used in the six-mask method. Diffusion forms most p-n junctions in the IC.

Figure II-2 illustrates the general case of diffusion: n-type impurities are present in a uniform concentration of 10^{20} atoms/cm^3. These diffuse into the still-solid p-type wafer, which had an initial impurity concentration of 10^{15} atoms/cm^3. It is intuitively obvious that diffusion depends on four factors:

(a) Type of impurity

(b) Amount of impurity

(c) Temperature (including room temperature)

(d) Time

The type of impurity determines the maximum concentration possible in solid silicon (called solid solubility), and how rapidly the impurity diffuses into the crystal (indicated by a parameter called the diffusion coefficient). It should be noted here that arsenic has a higher diffusion coefficient, and thus diffuses much more slowly, than phosphorus; both are, of course, n-type.

The amount of impurity present at the wafer surface is a boundary condition for the error-function diffused impurity curve; for example, referring again to Figure II-2, an increase in the diffusant concentration increases the diffused impurity level at a given depth, time and temperature. This then affects the junction location.

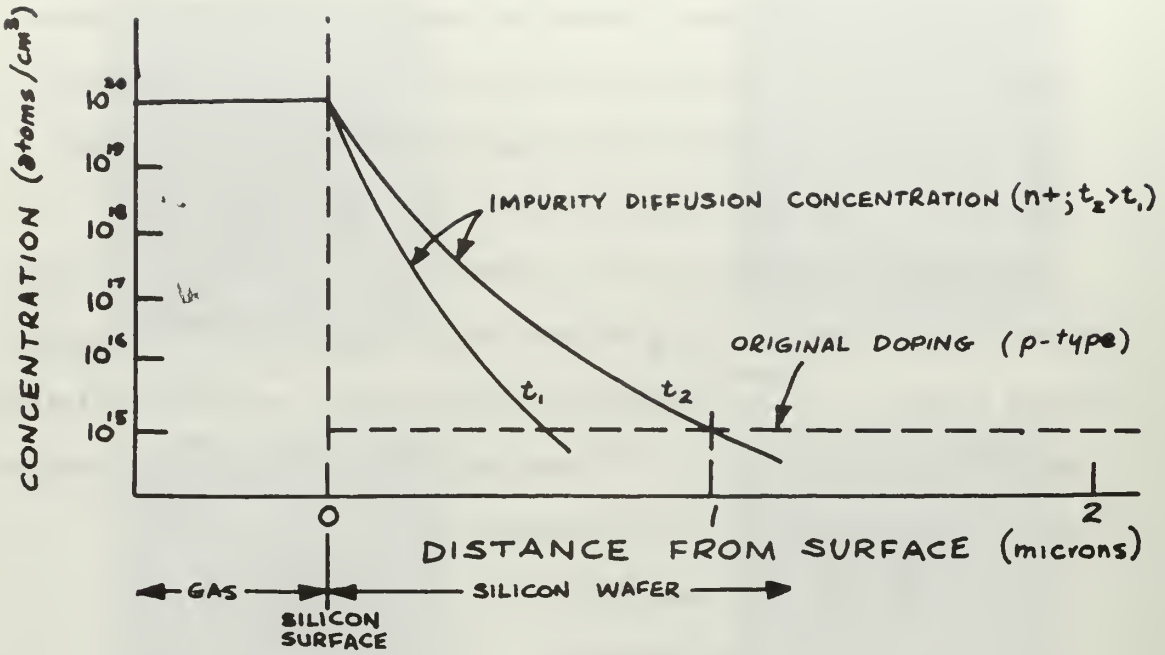


Figure II-2: Diffusion impurity concentrations.

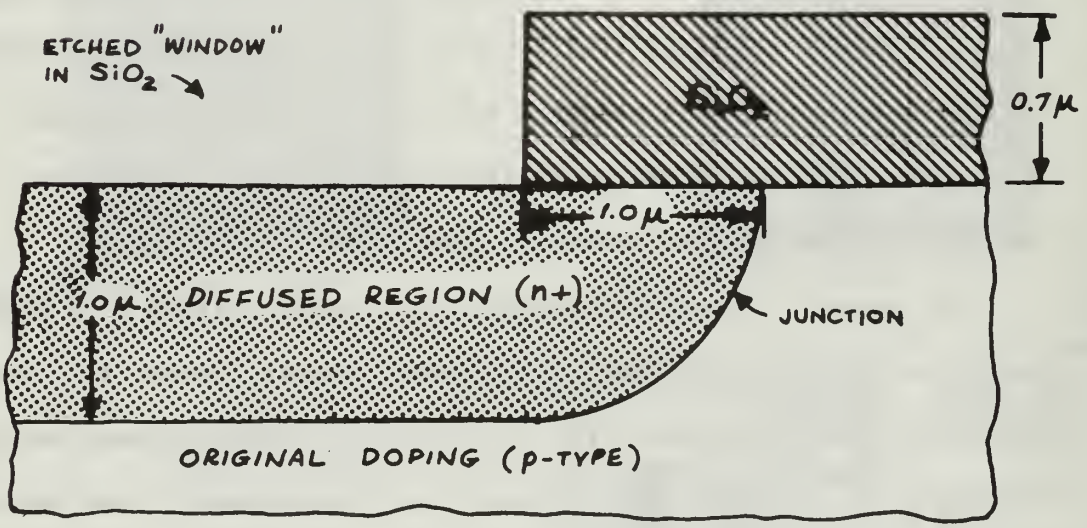


Figure II-3: Cross section of a diffused layer.

Temperature has a very strong effect on diffusion. Typically, the diffusion step in IC fabrication is made at 1200°C. Diffusion also occurs at room temperature, but is negligible. Not negligible, however is the further diffusion of previously added impurities when a wafer is reheated for subsequent diffusion; this must be considered in planning diffusion schedules.

Time is relatively easy to control; its effect is shown in Figure II-2.

Diffusion occurs about equally in all directions. The result is that in monolithic IC fabrication, impurities diffuse laterally as well as vertically, as shown in Figure II-3. This places junctions under the silicon dioxide layer, which provides the planar passivation.

The diffusions in a monolithic IC are typically shallow (on the order of microns) compared to mask dimensions (mils). This is because diffusion parameters can be more tightly controlled than the photo-masking and etching. Hence the lateral movement of impurities is much smaller than the size of the etched "window" in the silicon dioxide, controlled by the mask. This is why we stated previously that masks primarily control lateral dimensions of IC elements, and their location. Similarly, diffusion dictates the elements' vertical dimensions. Vertical tolerances are on the order of $\pm$ 10%.

As is demonstrated in the next section, the diffusion depicted in Figures II-2 and II-3 is that of the buried layer of our illustrative transistor.

It is of course desirable that a given impurity diffuse rapidly in Si, so that fabrication takes a reasonable length of time; it is also necessary that the impurity show negligible diffusion into SiO_2, so that the SiO_2 diffusion masking is possible. Boron and phosphorus meet both requirements; they are the most common impurities used. Because arsenic is masked by SiO_2, but diffuses slowly in Si, it is usually only used for an early diffusion that will not be affected much by later, shorter diffusions.

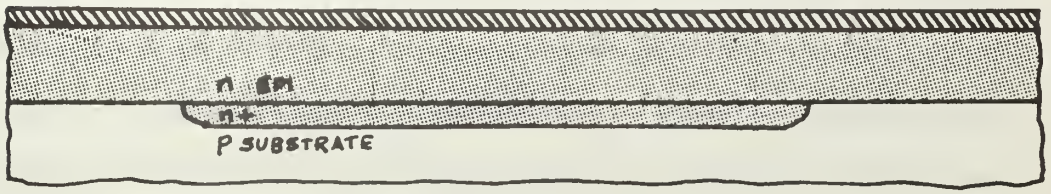
The Major Process Steps

Figure II-4 illustrates the following steps as applied to the fabrication of our illustrative transistor. The process begins with a 6 mil (about 150μ) monocrystalline Silicon wafer, which has been doped p-type to a resistivity of 10Ω-cm (about 10^{15} phosphorus atoms/cm^3). The six steps are:

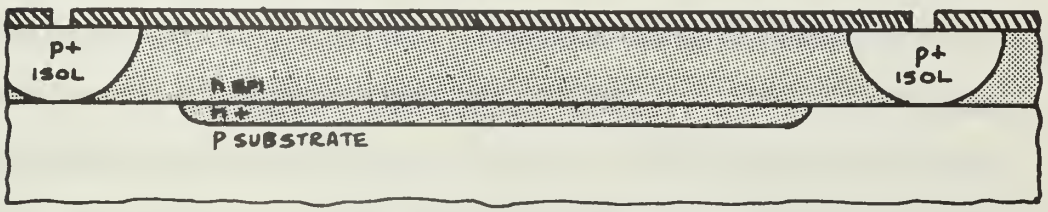
(a) Buried layer diffusion (Figure II-4(a)). The surface of the wafer is oxidized at about 1000°C; a layer of SiO_2 forms which is about .7μ thick. The oxide is then selectively etched away using the buried layer mask (Figure 1(a)), at locations where the buried layer is desired. An n-type diffusion, with surface concentration of 10^{20} arsenic atoms/cm^3, forms the n+ islands. Arsenic is used here as the diffusant so that the buried layers stay fairly fixed during later steps. The remaining SiO_2 is then removed by etching to prepare for the next step.

Monolithic IC transistors must have their collector contacts on top of the wafer. This means a long path for collector current through the high-resistivity epi collector; i.e., a large collector

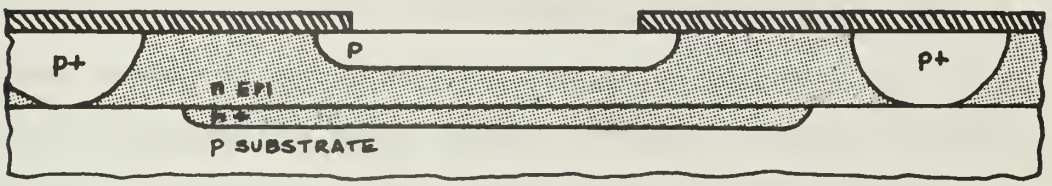
(a). Buried layer diffusion.



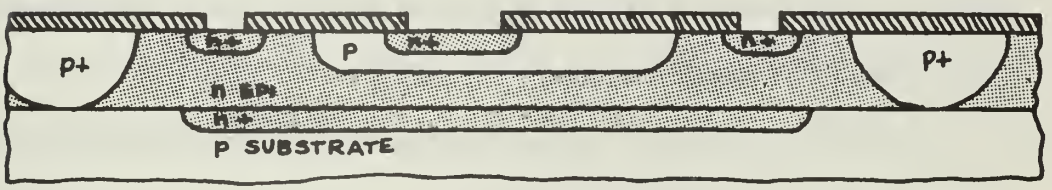
(b). Epitaxial growth.



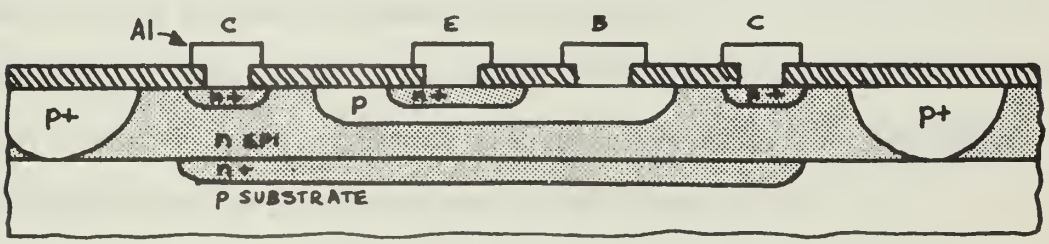
(c). Isolation diffusion.



(d). Base diffusion.



(e). Emitter diffusion.



(f). Metallization.

Figure II-4: Transistor example of monolithic IC fabrication. (Not to scale).

bulk resistance. This large resistance is undesirable in switching applications where it causes a high V_{CE} (sat); it is also undesirable, to a lesser extent, for its lowering of the transistors' frequency response. The high resistivity of the collector is necessary to ensure low C-B junction capacitance and high C-B junction breakdown voltage. However, the large bulk resistance can be reduced much as an order of magnitude by providing the buried n+ layer under the collector, which effectively parallels the collector bulk resistance with another, much smaller, resistor. With the buried layer, we still have a high resistivity collector in the vicinity of the junction, so the low junction capacitance and high junction breakdown voltage are retained.

(b) Epitaxial growth (Figure II-4(b)). A 1 mil (about 25μ) epitaxial layer is grown; this is n-type at .5Ω-cm resistivity (2×10^{17} boron atoms/cm^3). The epi layer resistivity is determined mainly by transistor requirements; this layer forms transistor collectors. The surface of the epi layer is then oxidized so that the entire wafer is again covered with SiO_2.

Prior to the use of epitaxially grown layers, there were two common methods of IC fabrication:

1. Diffused collectors, which meant base and emitter diffusions were made into a region of already graded profile, making junction locations very difficult to control; or

2. All diffused isolation, where the p-type isolation was diffused completely through the 5-6 mil n-type substrate, which meant a very long isolation diffusion time (diffusion times vary as the square of the diffusion depth).

Using the epi layer for collectors eliminated the problems associated with both of these previous methods.

Tolerances for modern epi fabrication are about the same as for diffusions: lower range resistivities can be controlled within $\pm$ 10%; thicknesses of 5-25μ within $\pm$ 10-20%.

(c) Isolation diffusion (Figure II-4(c)). The SiO_2 is selectively etched via the isolation mask (Figure II-1(b)), and a deep p+ diffusion (5 x 10^{20} boron atoms/cm^3) is made. This diffusion progresses across the epi layer to the substrate, so that wafer regions still covered by the SiO_2 are now isolated n-type islands, some with buried n+ layers. The isolation mask has thin opaque regions to reduce the lateral dimensions of the isolation diffusion. A layer of SiO_2 is again formed over the entire wafer surface.

(d) Base diffusion (Figure II-4(d)). The base diffusion mask (Figure II-1(c)) is used to control the selective etching. Then a shallow (3μ) p-type diffusion is made for transistor bases. This diffusion again uses boron donors, and has a 200Ω/square sheet resistance (about 10^{19} boron atoms/cm^3). The wafer surface is again oxidized.

(e) Emitter diffusion (Figure II-4(e)). The SiO_2 is again selectively etched, using the emitter diffusion mask (Figure II-1(d)). Then a shallow (2.2μ) n+ -type diffusion is made, using phosphorus acceptors with a sheet resistance of 2.1Ω/square (about 10^{21} phosphorus atoms/cm^3). This creates a base width of .8μ.

The same diffusion is used to form the top contacts for collectors. Aluminum is a p-type impurity in silicon, and the aluminum metallization

(step (g) below) introduces about 10^{18} aluminum atoms/cm^3 in the vicinity of aluminum-to-silicon contacts; this would create a rectifying contact (a pn junction), rather than the desired ohmic contact, if the aluminum were attached directly to the epi layer for collector contacts. However, the small n+ collector contacts formed by the emitter diffusion ensure ohmic contacts to the metallization, without appreciably affecting transistor performance.

The wafer is then again completely covered with SiO_2.

(f) Metallization (Figure II-4(f)). Before depositing the metallization, it is necessary to remove the SiO_2 insulating layer from the silicon wherever contacts to the IC elements are desired. This is done through selective etching using the contact holes mask (Figure II-1(e)).

Then the metallization overlay is formed by depositing evaporated aluminum over the entire wafer surface. This layer is the same thickness (0.7μ) as the SiO_2.

Finally the undesired aluminum is etched away, using the metallization mask (Figure II-1(f)).

The metallic film used must be a good conductor, make ohmic contacts with the IC elements, be reasonably easy to handle, adhere well to the SiO_2, and permit lead attachment. Aluminum is by far the most common metallization today, because it alone meets all of these requirements (with the use of n+ connector diffusions in high resistivity n-type regions, as mentioned earlier).

As with diffusion and epitaxy, metallization layers have tolerances on the order of 10%.

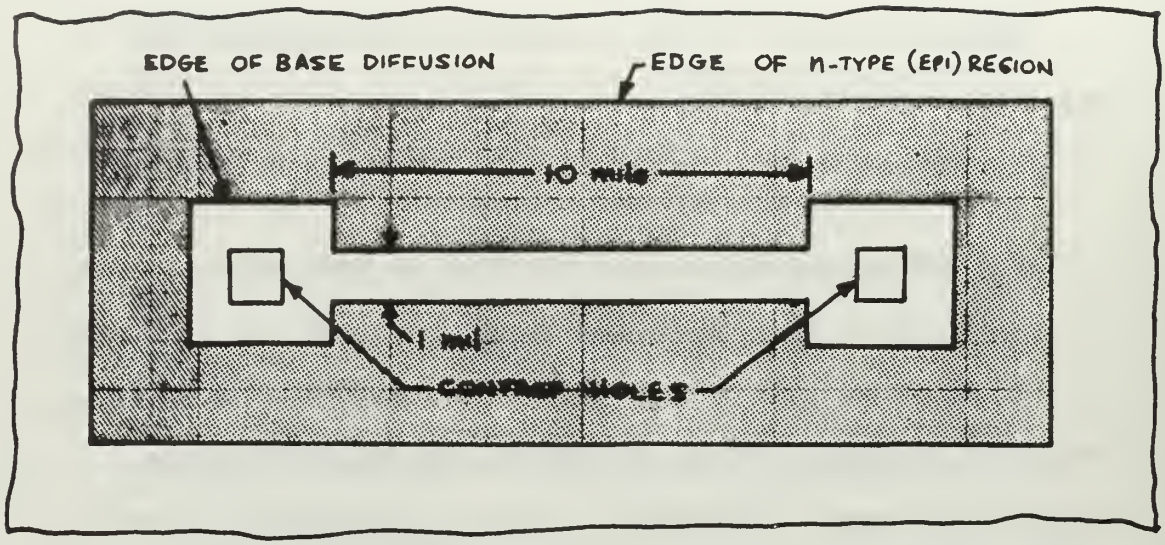
While Figure II-4 is not to scale, it does emphasize two significant fabrication facets:

1. Lateral dimensions are an order of magnitude greater than vertical ones; and
2. Diffusion moves as much laterally as vertically.

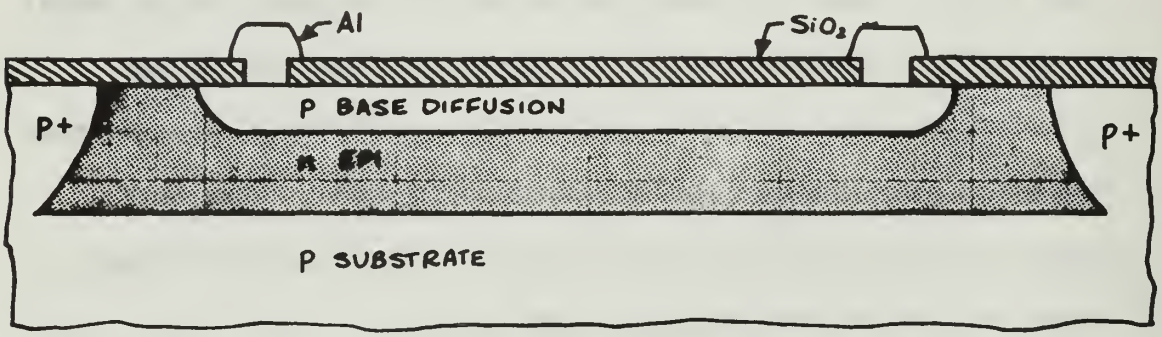
Completing the IC

In our integrated VFC, five types of components are needed. The first of these, the npn transistor, was described in the previous sections. In addition to the npn transistor, the VFC requires resistors, diodes, and pnp transistors. Conductor crossovers are also necessary. For economic reasons, these last four elements must be made using the standard npn transistor process steps (i.e., they must be compatible elements) if possible; any additional process steps would be very expensive. The methods for forming these four elements during standard processes are outlined below. Compatible capacitor values are too small to be useful in our VFC, so the fabrication of compatible capacitors is not discussed. Instead, we next consider the general problem of forming capacitors and inductors that are physically small. Then some aspects of diode isolation are mentioned. Finally, the remaining steps required to complete the IC are listed.

Resistors are usually made using the bulk resistance of regions formed by base (typically 200Ω/□) or emitter (about 2Ω/□) diffusions. Resistor values are controlled by resistor geometries. Figure II-5 shows a simple 2 KΩ geometry for a diffused resistor formed from the



(a). Geometry (top view).



(b). Cross section (vertical dimensions exaggerated).

Figure II-5: A diffused 2K ohm resistor.

200Ω/□ base diffusion; elementary calculations lead to its having a length/width ratio of 10/1. The geometry in Figure II-5 is actually an oversimplification, since the effects of the contact areas have been ignored; such effects are usually accounted for by empirical correction factors. The various processing tolerances lead to typical resistor value tolerances of 10-20%. However, for similar resistors which are close together, resistance ratios can be controlled within 3% or better. This is because processing errors tend to affect all resistors at the same time; for example, too long a base diffusion time means that all base diffusion resistors are formed from regions which are too deep.

Diodes are often realized by some configuration of the npn transistor; this scheme is usually more economical than forming special diode geometries. Of the five possible diode connections of the npn transistor, the base-emitter junction diode with the base-collector diode shorted has the lowest storage time and in general the least parasitic effects. This diode, shown in Figure II-6(a), is used throughout most of the integrated VFC. A roughly predictable breakdown voltage, on the order of 6.5 v, makes this diode useful for Zener diode applications, providing that the exact value of breakdown voltage is not a critical parameter. The catching diodes in the integrated VFC needed breakdown voltages in excess of 12 v however, so the diode in Figure II-6(a) could not be used. Instead, these two diodes used the base-collector junction, with the emitter-base junction shorted; this configuration, Figure II-6(b), has a reverse breakdown voltage well in excess of 30 v. Both diodes are formed by appropriate metallization over standard npn transistors.*

*For a much more complete discussion of the diode-connected transistor, see the 1963 report on this subject by H. C. Lin.[19]

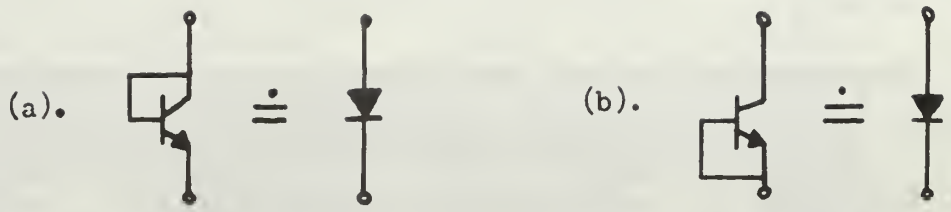
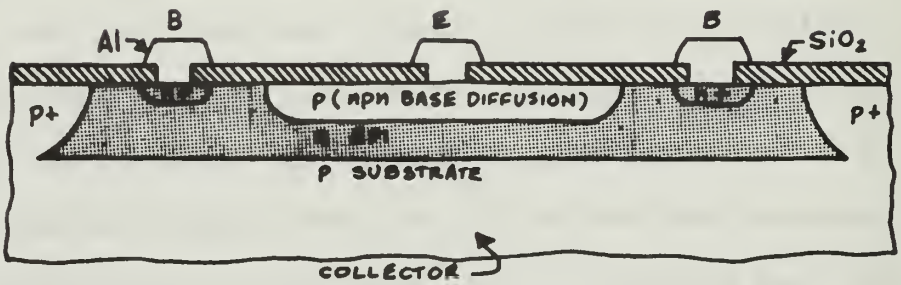
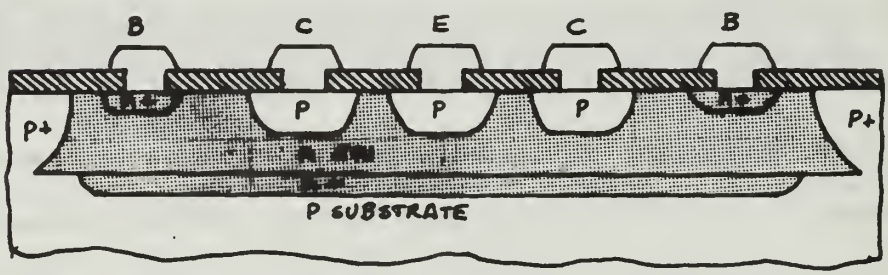


Figure II-6: Two diode-connected transistors.



(a). Vertical.



(b). Lateral.

Figure II-7: Compatible pnp transistors.
(Not to scale).

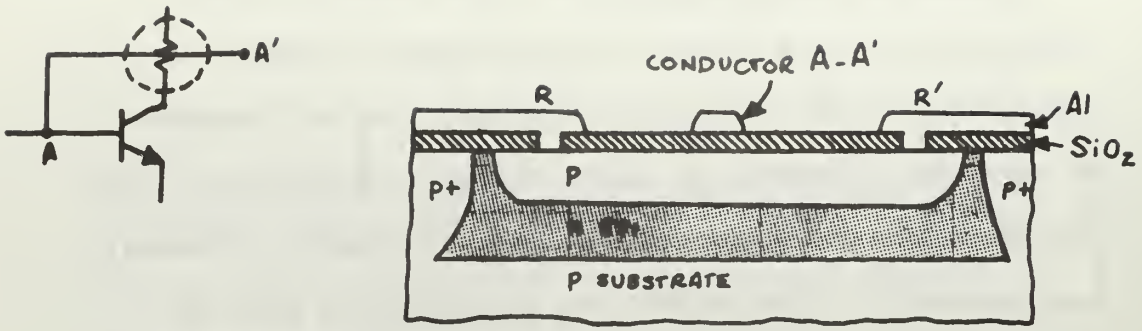
Compatible pnp transistors are often essential: pnp transistors are very useful in direct-coupled circuits, particularly in DC voltage level shifting; and the importance of compatibility should be clear. Figure II-7 illustrates the two compatible pnp structures available: vertical and lateral pnp transistors. Both suffer from wide bases; as might be expected, the vertical pnp transistor has typically a narrower base, and hence a higher (but still low) h_{FE}, than the lateral pnp transistor. The major disadvantage of the vertical pnp transistor is that its collector (the substrate) remains at a constant voltage, as explained below. Hence the vertical pnp transistor is limited to emitter-follower (common collector) applications. In both types of compatible pnp transistors, the low h_{FE} problem may be circumvented by driving the pnp transistor with an npn transistor.*

Crossovers (points where one conductor must cross over another) are necessary in virtually all monolithic IC's. There are three common methods of forming crossovers:

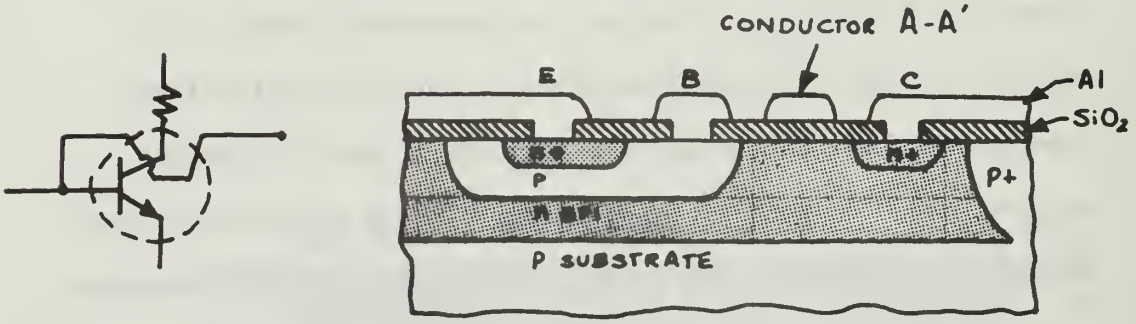
1. Metallization conductor over a diffused resistor;
2. Metallization conductor over an extended transistor, which increases the transistor's collector bulk resistance; and
3. Metallization conductor over a diffused (n+) conductor.

These methods are listed above in order of preference, and are shown in Figure II-8 for a hypothetical circuit. All three methods introduce

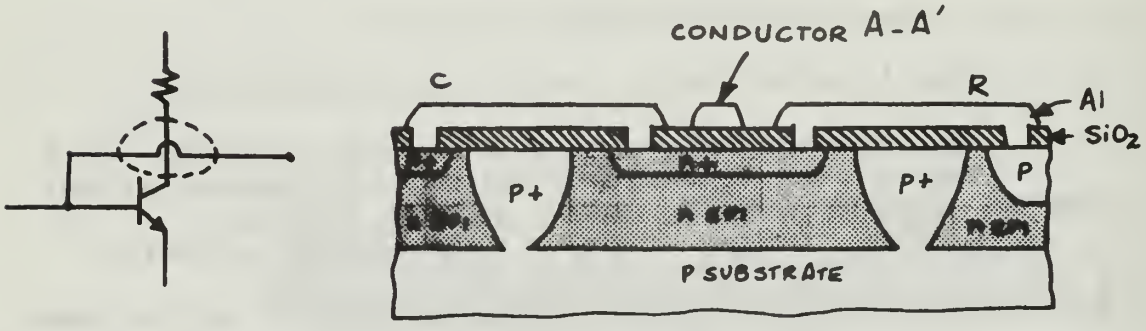
*The lateral pnp transistor, and a compound-connected npn-pnp transistor pair which approximates a high h_{FE} pnp transistor using the compatible lateral pnp transistor are described Lin, et al.[20]



(a). Metal over diffused resistor.



(b). Metal over collector.



(c). Metal over diffused conductor.

Figure II-8. Three approaches to a crossover.
(Not to scale; buried layer omitted).

parasitics and increase the IC complexity and area; crossovers are to be avoided wherever possible.

Capacitors and inductors are not amenable to integration, due solely to the small physical dimensions of IC's. Compatible capacitors have been fabricated, using SiO_2 as the dielectric, but these have values on the order of 0.3 pf/mil^2 which makes them too small for most uses.[21] Inductors are impossible to fabricate in a monolithic IC: if a given inductor is scaled down in size by some scale factor, not only does inductance decrease by the same scale factor, but also the series resistance, so that Q_L decreases as the square of the scale factor.[22]

Isolation in monolithic IC's is most often accomplished by reverse biasing of the component-to-substrate and component-to-isolation diffusion junctions. For instance, the diffused resistor of Figure II-5 could be isolated by insuring that the epi region was always at a higher potential than the substrate. If the substrate is kept at the lowest potential in the IC, as is usually the case, then all such isolation diodes will be reverse biased, or at least never forward biased. Experience has shown that proper use of diode isolation has virtually eliminated interaction of IC elements; leakage currents are negligible and parasitic effects essentially only limit bandwidth.[23-25]

Following the batch fabrication outlined above, monolithic IC's are tested on the wafer. Then the wafer is separated into the individual dice for further testing and packaging. The packaging at present is the most costly step in monolithic IC

production, and is inefficient from a volume standpoint: at best, an IC chip ends up in a package about 2000 times as large as the chip.[26]

Cost Considerations

One of the most important parameters of any electronic device is its cost, and monolithic IC's are no exception.

A large amount of the unit cost of an assembled monolithic IC lies in its package; for example, the relatively cheap TO-5 type package at about 15 cents may be twice as expensive as the chip it encloses. Getting the chip into its package, and the necessary testing before and after packaging, further increase the unit cost. These considerations are outside the scope of this paper.

The cost of the chip itself is equally important; it is this cost which makes the monolithic IC technology not only feasible but dominant. Other costs, such as packaging, are high only by comparison. There is one primary rule-of-thumb: all wafers cost about the same to process. The typical monolithic IC production line uses the same diffusion schedule to produce all its IC's; all that changes for different types of IC's are the masks used. This means that overall IC area and process yield become very important. The smaller the area of an IC, the more IC's can be produced on a single wafer. And the higher the yield, the more of these IC's are usable.

IC area is controlled by a mix of circuit design and mask layout. The need for minimizing IC area dictates some unusual design constraints. For instance, the 2 KΩ diffused resistor in

Figure II-5 had a surface area of 150 mil^2, which is five times the area occupied by our illustrative transistor. Clearly the total amount of resistance in an IC must be kept to a minimum, and resistors should be replaced by transistors (or transistors and smaller resistors) wherever possible. Mask layout is a job for experienced experts; in passing, let us only note that grouping IC elements in a single isolation region can be an excellent method for conserving IC area.

Yield is a complicated function of many variables. It might appear that if we are interested in decreasing the cost per circuit function, then we should make IC's as complex as possible to place as many functions as possible within the inherently expensive package. However, it has been discovered that increasing IC complexity (and hence IC area) produces a rather dramatic decrease in yield; there appears to be an optimum number of elements per IC in terms of unit cost. One factor here is that a larger IC area increases the probability that the IC will lie on a wafer defect, and thus be unacceptable. Maximum bipolar monolithic IC area is typically 60 mils square.

Yield is also a sensitive function of IC specifications; too demanding specifications can make most IC's unacceptable. And finally, good circuit design can strongly improve yield by reducing the effect of IC element variations on the IC's overall performance. Yield is, like mask details and diffusion schedules, a very tightly held secret of the IC manufacturer; however, ICE's Madland states

that 1% was the 1966 average for monolithic IC's,[27] and, as a more recent example, estimates a 10% monolithic IC yield for RCA in late 1967.[28]

A typical two inch diameter wafer might have cost fifty cents to prepare. Epitaxy, diffusions, and other production costs might raise the direct cost of the wafer to about $25. About 1,250 50 mils square IC's can be formed on the wafer. That means that the direct cost per chip, before packaging, would be about $2.00 for a 1% yield and about $.20 for a 10% yield.

The initial costs of any monolithic IC are high. A set of masks costs thousands of dollars. Much time and effort goes into circuit design and optimization, and a continuing, expensive research and development effort must accompany any competitive IC manufacturing. This means that monolithic IC's are cheap only if their high initial costs can be amortized in slight unit cost increments for very large volume production. Hence any monolithic IC is usually designed for a large market appeal: most linear IC's, for instance, are general purpose designs.

Moreover, the market appeal of monolithic IC's depends largely on their achieving many circuit functions per chip, so designs usually maximize function density on the chip by incorporating small area components: transistors, diodes, and small resistors are used, but not capacitors or large resistors.

The preceding discussion points out the major disadvantage of monolithic IC's, as compared to other IC technologies: lengthy, expensive pre-production activity (design, optimization, and mask

making). IC's which require rapid progression from inception to production, or which require moderate unit prices for small quantities, must come from some technology other than monolithic. For instance, in a recent report engineers from the Navy Underwater Sound Laboratory described their search for a suitable microelectronic preamplifier for use with hydrophone transducers.[29] In addition to circuit performance disadvantages, the requisite long and expensive development ruled out monolithic IC's from consideration; a hybrid IC was the final choice.

The optimum IC, from economic factors, is the IC which delivers the most circuit functions per unit cost. However, some circuit functions, such as large capacitance, are prohibitively expensive to integrate in monolithic form, and others, such as inductance, are practically impossible. The logical approach is to integrate only those functions which lend themselves readily to monolithic construction, such as transistors with their biasing networks, and use external discrete components as required to realize a desired overall circuit function. This approach is especially necessary in linear circuits, where standard IC production must be applied to a large number of different circuit function requirements, each with a relatively small market.[30]

INITIAL DISTRIBUTION LIST

		No. Copies
1.	Defense Documentation Center Cameron Station Alexandria, Virginia 22314	20
2.	Library Naval Postgraduate School Monterey, California 93940	2
3.	Commandant of the Marine Corps (Code A03C) Headquarters, U. S. Marine Corps Washington, D. C. 22214	1
4.	Professor R. Panholzer Department of Electrical Engineering Naval Postgraduate School Monterey, California 93940	2
5.	Professor William M. Bauer Department of Electrical Engineering Naval Postgraduate School Monterey, California 93940	1
6.	Professor George J. Thaler Department of Electrical Engineering Naval Postgraduate School Monterey, California 93940	1
7.	Capt. J. H. Wickens, USMC c/o Dr. C. R. White 1461 Lone Oak Drive Macon, Georgia 31201	4
8.	Dr. John R. Hulme Fairchild Semiconductor 313 Fairchild Drive Mountain View, California 94041	1
9.	Mr. Murray Siegel Fairchild Semiconductor 313 Fairchild Drive Mountain View, California 94041	1
10.	Mr. Mike J. Cochran Cintra Data Systems 711 Eunice Avenue Mountain View, California 94041	1

11. LT Richard M. Akita, USN — 1
c/o Mr. Glen Tateno
45-880 Keneke Street
Kaneohe, Hawaii 96744

12. LT Robert C. McFarland, USCG — 1
SMC 1680
Naval Postgraduate School
Monterey, California 93940

13. LT Garland F. Skinner, USN — 1
SMC 1443
Naval Postgraduate School
Monterey, California 93940

DOCUMENT CONTROL DATA - R & D

Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1 ORIGINATING ACTIVITY (Corporate author)
Naval Postgraduate School
Monterey, California 93940

2a. REPORT SECURITY CLASSIFICATION
Unclassified

2b. GROUP

3 REPORT TITLE

An Integrated Voltage-to-Frequency Converter: A Tutorial Design Study of a New Monolithic Integrated Circuit

4 DESCRIPTIVE NOTES (Type of report and, inclusive dates)
Thesis, June 1968

5 AUTHOR(S) (First name, middle initial, last name)
Justin H. Wickens

6 REPORT DATE
June 1968

7a. TOTAL NO. OF PAGES
159

7b. NO. OF REFS
208

8a. CONTRACT OR GRANT NO.

b. PROJECT NO.

c.

d. Distribution unlimited

9a. ORIGINATOR'S REPORT NUMBER(S)

9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)

10 DISTRIBUTION STATEMENT

This document is subject to special export controls and each transmittal to foreign government or foreign nationals may be made only with prior approval of the Naval Postgraduate School.

11 SUPPLEMENTARY NOTES

12. SPONSORING MILITARY ACTIVITY
Naval Postgraduate School
Monterey, California 93940

13 ABSTRACT

Engineers throughout the electronics industry must understand the details of integrated circuit (IC) design, so that they can recognize possible IC applications, evaluate existing IC's, and, at times, even design new IC's. In particular, they must understand monolithic IC design, since the monolithic IC is the most prevalent IC today, and typifies IC design problems.

This thesis provides a complete introduction to monolithic IC design: circuit selection, circuit design, and circuit evaluation are discussed. Fabrication information and terminology are included as appendices. The corresponding design phases of a new IC -- the integrated voltage-to-frequency converter (VFC)--are discussed in each section of the thesis, to illustrate the applications of the various design principles. This integrated VFC, designed by the author, is shown to be a feasible monolithic IC design.

14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Integrated Circuit						
Integrated Circuit Design						
Integrated Voltage-to-Frequency Converter						
Monolithic Integrated Circuit						
Monolithic Integrated Circuit Design						
Voltage-Controlled Oscillator						
Voltage-to-Frequency Converter						